PNX8526 Reg. Summary List AN10263_1

Programmable Source Decoder with Integrated Peripherals

Rev. 01 — 8 October 2003

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PHILIPS

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Chapter 1: RSL Overview

Programmable Source Decoder with Integrated Peripherals

Rev. 01 — 8 October 2003

1.1 Register Summary List (RSL)

The tables in the RSL (Chapters 2 to 6), provide the following register information for the PNX8526:

- The Module name is identified at the top of each table. Next to it is the Reference where more detail about those registers can be found.
- Each shaded row contains a register offset (address) and name. Offsets are listed in ascending order (0 to n).
- Bits used in a described function are listed in descending order from 31 to 0.
- Read/write characteristic of each bit is noted.
- *Reset value of a register field is noted.
- A brief description of the register/bits is provided.

* The reset value reflects the bit value immediately following start up or system reset. The letters **NI** in this column indicate “Not Initialized.” This means the register is not initialized and may contain random data.

The following definitions apply to “Reserved”, “Unused” and “R/W” bits listed in the RSL.

- **Reserved** These bits are undefined and should not be written to.
- **Unused** These bits can be written or read, but have no effect on any part of the PNX8526. **There is no guarantee that data written to these bits will be stored.**
- R = Read Only: This bit can only be read. Writing to this bit will not affect the functionality. Typically this is used for status indication.
- W = Write Only: Writing to this bit will affect functionality. Contents read back from this bit may not contain valid information.
- R/W = Read and Write: This bit can be read and written. Both reading and writing will affect the functionality.

Table 1 includes the base address and reference page number for the PNX8526 registers. Registers are presented in numerical order by offset. Check the page number beside each module name for its location in this book.

Table 1: Aperture Map for PNX8526 Database

Status	Aperture Start	Aperture Size	Module Name	Page Reference
Fixed Address				
Ch 38 EJTAG-probe*	0xFF20 0000	1 M	MIPS E-JTAG Software Debug Port	
Ch 24 PR3940*	0xFF30 0000	1 M	Internal MIPS Processor	
PCI Configuration				
Ch 8 PCI	Not Applicable		PCI Configuration Registers	page 2-4
Relocatable Memory Mapped				
F-Default Slv	0x00 0000	244K	Reserved	
EJTAG	0x03 D000	4K		
Ch 6 M-PIC	0x03 E000	4K	Interrupts	page 2-10
Ch 35 FPBC	0x03 F000	4K	PI-Bus Arbiter	page 2-15
Ch 8 PCI/XIO	0x04 0000	4K	PCI-XIO	page 2-20
SPY Micro-Architecture Supplement	0x04 1000	4K	SPY Debug	page 2-32
Ch 3 Boot	0x04 2000	4K	Boot Module	page 2-38
Ch 16 Smart1	0x04 3000	4K	Smartcard UART	page 2-38
Ch 16 Smart2	0x04 4000	4K	Smartcard UART	page 2-48
Ch 15 IIC1	0x04 5000	4K	I^2C Ports	page 2-49
Ch 15 IIC2	0x04 6000	4K	I^2C Ports	page 2-53
Ch 5 Clocks	0x04 7000	4K	Clock, Reset & Power Management	page 2-53
Ch 13 USB	0x04 8000	4K	USB Port	page 3-76
Ch 14 1394	0x04 9000	4K	IEEE 1394	page 3-82
Ch 11 UART1	0x04 A000	4K	UART Ports	page 3-102
Ch 11 UART2	0x04 B000	4K	UART Ports	page 3-108
Ch 11 UART3	0x04 C000	4K	UART Ports	page 3-108
Global Regs 2	0x04 D000	8K		page 3-109
Ch 35 MPBC	0x04 E000	4K	PI-Bus Arbiter	page 3-123
Ch 29 D2D	0x04 F000	68K	2D Drawing Engine	page 3-126
Ch 5 Reset	0x06 0000	4K	Clock, Reset & Power Management	page 3-134
Ch 39 TMDBG	0x06 1000	4K	TM32 JTAG Software Debug Port	page 3-135
Ch 32 CRC Check Coprocessor	0x06 2000	4K	DMA Controller	page 3-137
Global Regs 1	0x06 3000	4K		page 3-141
M-Default Slv	0x06 4000	624K	Reserved	
Ch 25 TM32	0x10 0000	8K	Internal TM32 Media Processor	page 4-144
Ch 6 T-PIC	0x10 2000	4K	Interrupts	page 4-155
Ch 35 TPBC	0x10 3000	4K	PI-Bus Arbiter	page 4-159
Ch 10 GPIO	0x10 4000	4K	GPIO/IR	page 4-163
Ch 34 MPG	0x10 5000	4K	MPEG & Video Decoder	page 4-180

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Table 1: Aperture Map for PNX8526 Database

Status	Aperture Start	Aperture Size	Module Name	Page Reference
Ch 26 VIP1	0x10 6000	4K	VIP	page 4-190
Ch 26 VIP2	0x10 7000	4K	VIP	page 4-202
Ch 12 SSI	0x10 8000	4K	SSI Port	page 5-205
Ch 23 SPDIFOUT	0x10 9000	4K	SPDIF Output Port	page 5-211
Ch 22 SPDIFIN	0x10 A000	4K	SPDIF Input Port	page 5-213
Ch 27 MBS	0x10 C000	4K	MBS	page 5-220
T-Default	0x10 D000	4K	Reserved	
Ch 28 AICP1	0x10 E000	4K	AICP	page 5-234
Ch 28 AICP2	0x10 F000	4K	AICP	page 5-250
Ch 21 AOUT1	0x11 0000	4K	Audio (I^2S) Output Ports	page 6-252
Ch 20 AIN1	0x11 1000	4k	Audio (I^2S) Input Ports	page 6-256
Ch 21 AOUT2	0x11 2000	4K	Audio (I^2S) Output Ports	page 6-259
Ch 20 AIN2	0x11 3000	4K	Audio (I^2S) Input Ports	page 6-259
Ch 21 AOUT3	0x11 4000	4K	Audio (I^2S) Output Ports	page 6-260
Ch 20 AIN3	0x11 5000	4K	Audio (I^2S) Input Ports	page 6-261
Ch 31 TSDMA	0x11 6000	4K	Software Transport Stream	page 6-261
T-Default	0x11 7000	4K	Reserved	
Ch 33 MSP1	0x11 8000	32K	MSP	page 6-266
Ch 33 MSP2	0x12 0000	32K	MSP	page 6-283
T-Default	0x12 8000	864K	Reserved	

1.2 Offsets

The RSLs list offsets in ascending order. The offsets are also identified by their register module name as shown in Table 1 above.

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PCI Configuration Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.8)

PCI CONFIGURATION REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x0000			***Device ID/Vendor ID***	
31:16	R	0x8500	Device ID	The ID assigned by the PCI SIG representative. The value will be hard coded. Reset value 8500 has been assigned to the PNX8526.
15:0	R	0x1131	Vendor ID	Value 0x1131 is the ID assigned to Philips Semiconductors by the PCI SIG representative.
Offset 0x0004			***Command/Status***	
31	R/W	0	Parity Error	This bit will be set whenever the device detects a parity error. Write 1 to clear.
30	R/W	0	Signaled System Error	This bit is set whenever the device asserts SERR. Write 1 to clear.
29	R/W	0	Received Master Abort	Set by the PCI master when its transaction is terminated with a master abort. Write 1 to clear.
28	R/W	0	Received Target Abort	Set by the PCI master when its transaction is terminated with a target abort. Write 1 to clear.
27	R/W	0	Signaled Target Abort	Set by the PCI target when it terminates a transaction with a target abort. Write 1 to clear.
26:25	R	01	Devsel Timing	The PCI target uses medium DEVSEL timing.
24	R/W	0	Master Data Parity Error	Set by the PCI master when PERR is observed.
23	R	1	Fast Back-to-Back Capable	The PCI supports fast back-to-back transactions.
22	R	0	Reserved	
21	R	cfg*	66 MHz Capable	0 = 33 MHz PCI (PNX8526 is 33 MHz). *Value determined by PCI Setup register.
20	R	1	Capabilities List	Indicates a new Capabilities linked list is available at offset 40h.
19:10	R	0000	Reserved	
9	R/W	0	Fast back-to-back enable	Enable fast back-to-back transactions for PCI master.
8	R/W	0	SERR enable	Enable SERR to report system errors.
7	R	0	Stepping Control	Address stepping is not supported.
6	R/W	0	Parity Error Response	0 = No parity error response 1 = Enable parity error response.

PCI CONFIGURATION REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
5	R	0	VGA Palette Snoop	VGA is not supported.
4	R/W	0	Memory Write & Invalidate	Enable use of memory write and invalidate.
3	R	0	Special Cycles	Special cycles are not supported.
2	R/W	0	Enable Bus Master	Enable the PCI bus master.
1	R/W	0	Enable Memory space	Enable all memory apertures.
0	R	0	Enable IO Space	The PNX8526 does not respond to IO transactions.
Offset 0x0008			***Class Code/Revision ID***	
31:8	R/W*	0x040000	Class Code	The PNX8526 is defined as a multimedia video device. *The boot loader may change the class code to an alternate value if done before writing to the pci_setup register.
7:0	R	1	Revision ID	Revision ID. Will initially be assigned to 0. Revision ID must not be synthesized. It will need to be changed with revised silicon, whether for bug fixes or enhancements.
Offset 0x000C			***Latency Timer/Cache Line Size***	
31:16	R	0x0000	Reserved	Note: BIST is not implemented. Header is 0.
15:8	R/W	0	Latency Timer	Latency Timer
7:0	R/W	0	Cache Line Size	Cache Line Size
Offset 0x0010			***Base10 Address Register***	
This aperture is for the SDRAM on the PNX8526. 64M, 32M or 16M memory sizes are supported on the PNX8526.				
31:28	R/W	0	Base10 Address	Upper 4 bits of base10 address of the first memory aperture
27:21	R/W*	0	Base10 Address	*The base 10 can be configured to various aperture sizes from 2 MB to 256 MB. (See Offset 0x04 0010 PCI Setup on page 2-23). Depending on aperture size selected, various bits will be R/W or Read Only. Bit: 27262524232221 256M:RORORORORORORO 128M:RWRORORORORORO 64M:RWRWRORORORORO 32M:RWRWRWRORORORO 16M:RWRWRWRWRORORO 8M:RWRWRWRWRWRORO 4M:RWRWRWRWRWRWRO 2M:RWRWRWRWRWRWRW
20:4	R	0	Reserved	
3	R	cfg	Prefetchable	Value is determined at boot time.
2:0	R	0	Type	Indicates type 0 memory space (locatable anywhere in 32-bit address space).
Offset 0x0014			***Base14 Address Register***	
This aperture will be set to 2 MB for MMIO on the PNX8526.				
31:28	R/W	0001	Base14 Address	Upper 4 bits of base14 address of the first memory or IO aperture

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PCI CONFIGURATION REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
27:21	R/W*	1011111	Base14 Address	*The base 14 can be configured to various aperture sizes from 2 MB to 256 MB. (See Offset 0x04 0010 PCI Setup on page 2-23). Depending on aperture size selected, various bits will be R/W or Read Only. **Bit: 27262524232221** 256M:RORORORORORORO 128M:RWRORORORORORO 64M:RWRWRORORORORO 32M:RWRWRWRORORORO 16M:RWRWRWRWRORORO 8M:RWRWRWRWRWRORO 4M:RWRWRWRWRWRWRO 2M:RWRWRWRWRWRWRW
20:4	R	0	Reserved	
3	R	cfg	Prefetchable	Value is determined at boot time.
2:0	R	0	Type	Type of aperture. 0 = PCI type 0 1 = PCI type 1 Indicates type 0 memory space (locatable anywhere in 32-bit address space).
Offset 0x0018			***Base18 Address Register***	
This aperture is for the XIO on the PNX8526, which supports up to 128 MB of XIO memory space.				
31:28	R/W	0001	Base18 Address	Upper 18 bits of base address of the first memory or IO aperture
27:21	R/W*	1100000	Base18 Address	*The base 18 can be configured to various aperture sizes from 2 MB to 256 MB. (See Offset 0x04 0010 PCI Setup on page 2-23). Depending on aperture size selected, various bits will be R/W or Read Only. **Bit: 27262524232221** 256M:RORORORORORORO 128M:RWRORORORORORO 64M:RWRWRORORORORO 32M:RWRWRWRORORORO 16M:RWRWRWRWRORORO 8M:RWRWRWRWRWRORO 4M:RWRWRWRWRWRWRO 2M:RWRWRWRWRWRWRW
20:4	R	0	Reserved	
3	R	cfg*	Prefetchable	Prefetchable if configured as 1. *Value determined by PCI Setup register.
2:0	R	0	Memory	This bit indicates type 0 memory aperture.
Offset 0x002C			***Subsystem ID/Subsystem Vendor ID***	
The values used in this register will be loaded into the register before entertaining any transactions on the PCI bus. The boot loader will initialize control register address 0x006C with the correct values.				
31:16	R	0	Subsystem ID	Subsystem ID. The value for this field is provided by Philips PCI SIG representative for Philips internal customers. External customers will provide their own number.

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PCI CONFIGURATION REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
15:0	R	0	Subsystem Vendor ID	Subsystem Vendor ID. The value for this field is 1131 for Philips internal customers. External customers need to apply to the PCI SIG to obtain a value if they do not have one already.
Offset 0x0030			***Reserved***	
Offset 0x0034			***Capabilities Pointer***	
31:8	R	0	Reserved	
7:0	R	0x40	cap_pointer	Indicates extended capabilities are present starting at 40.
Offset 0x003C			***Max_Lat, Min_Gnt, Interrupt pin, Interrupt Line***	
31:24	R	0x18	max_lat	Indicates the max latency tolerated in 1/4 microsecond for PCI master.
23:16	R	0x09	min_gnt	Indicates how long the PCI master will need to use the bus.
15:8	R	0x01	interrupt_pin	Indicates which interrupt pin is used.
7:0	R/W	0x00	interrupt_line	Interrupt routing information
Offset 0x0040			***Power Management Capabilities***	
31:27	R	0x0000	Reserved	
26	R	cfg*	d2_support	1 = Device supports D2 power management state *Value determined by PCI Setup register.
25	R	cfg*	d1_support	1 = Device supports D1 power management state *Value determined by PCI Setup register.
24:19	R	0	Reserved	
18:16	R	010	version	Indicates compliance with version 1.1 of PM.
15:8	R	00	Next Item Pointer	There are no other extended capabilities.
7:0	R	01	Cap_ID	Indicates this is power management data structure.
Offset 0x0044			***PMCSR***	
31:2	R		Reserved	
1:0	RW		pwr_state	power_state

FPI Null Module Registers.

FPI NULL MODULE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x00 0FFC			***Module ID Register***	
31:16	R	0x0124	MOD_ID	Module ID Number
15:12	R	0	REV_MAJOR	Major revision
11:8	R	0	REV_MINOR	Minor revision
7:0	R	0x3C	APP_SIZE	Aperture size is 0 = 4 kB.

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MIPS E-JTAG S'ware DeBug Port Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.38)

MIPS E-JTAG SOFTWARE DEBUG PORT REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x03 D000			***Implementation Register***	
31:26	R		reserved	
25:24	R		ProfSup	PROFILINGsUPPORT: Defines if profiling is supported. 00 No profiling support. 01 Simple DMA profiling supported. 10,11 Reserved.
23	R		SDBBPCode	3$""0USES3PECIAL_/PCODE_FOR-)03)_))_))_)6 0: SDBBP is encoded according to 1.3 specification 1: SDBBP is encoded using a Special2 Opcode
22:21	R		ASIDsize	3IZEOF!3)$FIELDINIMPLEMENTATION: Defines the size of the ASID in the implementation: 00 No ASID in implementation. 01 6 bit ASID. 10 8 bit ASID. 11 Reserved.
20	R		CplxBrk	#OMPLEX"REAK3UPPORT_ This bit is set to '1' when Complex Break is supported, and otherwise set to '0'.
19	R		PhysAW	0HYSICAL!DDRESS7IDTH Informs the size of EJTAG_Address_register 0: Physical addresses are 32-bit in length 1: Physical addresses is from 33 to 64-bits in length The exact length of can be determined by shifting a pattern through the EJTAG Address Register.
18	R		DCacheC	$ATA#ACHE#OHERENCY 0: Data Cache does not keep coherency with DMA 1: Data Cache keeps coherency with DMA
17	R		ICacheC	)NSTRUCTION#ACHE#OHERENCY 0: Instruction Cache does not keep DMA coherency 1: Instruction Cache keeps coherency with DMA
16	R		MIPS16	-)03__3UPPORT 0: MIPS CPU does not support MIPS16 1: MIPS CPU supports MIPS16
15	R		NoPCTrace	.O0#4RACE3UPPORT 0: PC Trace is supported by implementation 1: PC Trace is not supported by implementation

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MIPS E-JTAG SOFTWARE DEBUG PORT REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
14	R		NoDMA	.O%*4!'$-!3UPPORT 0: EJTAG DMA is supported by implementation 1: EJTAG DMA is not supported by implementation
13:11	R		TPCW	40#7IDTH 000,111 1 bit 000 is Standard EJTAG 001 2 bits Extended EJTAG 010 4 bits Extended EJTAG 011 8 bits Extended EJTAG others reserved Extended EJTAG
10:8	R		PCSTW	0#347IDTHAND$#,+$IVISION&ACTOR 000,111 3 bits (DCLK is 1/1 of MIPS CPU CLK) 001 6 bits (DCLK is 1/2 of MIPS CPU CLK) 010 9 bits (DCLK is 1/3 of MIPS CPU CLK) 011 12 bits (DCLK is 1/4 of MIPS CPU CLK) others reserved Note: 000 is for standard EJTAG, the other values for the Extended EJTAG.
7	R		NoProcBrk	0ROCESSOR"US"REAK: this bit indicates if the Processor Bus Break function is implemented in the DSU. 0: Processor Bus Break is implemented 1: Processor Bus Break is not implemented
6	R		NoDataBrk	$ATA!DDRESS"REAK: this bit indicates if the Data Ad-dress Break function is implemented in the DSU. 0: Data Address Break is implemented 1: Data Address Break is not implemented
5	R		NoInstBrk	)NSTRUCTION!DDRESS"REAK: this bit indicates if the Instruction Address Break function is implemented in the DSU. 0: Instruction Address Break is implemented 1: Instruction Address Break is not implemented
4:1	R		Ch[3:0]	/BSOLETEFIELD: debug SW should check InstrBrk, DataBrk and ProcBrk to know what break types are implemented. .UMBEROF"REAK#HANNELS: these 4 bits used to indicate the number of break channels implemented in the DSU. 0000 = no break channels 0001 = 1 break channel ... 1111 = 15 break channels

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MIPS E-JTAG SOFTWARE DEBUG PORT REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
0	R		MIPS32/64	-)03__ BITOR__ indicates the type of MIPS CPU, in-forming the width of the MIPS CPU datapath, the de-bug registers implemented in the DSU, and the EJTAG_Data_register. 0: 32-bit wide data registers 1: 64-bit wide data registers
Offset 0x03 DFFC			***Module ID***	
31:16	R	0x0104	MODULE_ID	Module ID Number
15:12	R	0	REV_MAJOR	Major Revision
11:8	R	0	REV_MINOR	Minor Revision
7:0	R	0	APP_SIZE	Aperture Size is 0 = 4 kB.

Priority Interrupt Controller (M-Pic) Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.6)

PRIORITY INTERRUPT CONTROLLER (M-PIC) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x03 E000			***PIC_INT_PRIORITY***	
31:4		-	Unused	Read as zero
3:0	R/W	0xF	PRIORITY_LIMITER	Interrupt Priority Limiter: Pending Interrupts with priority greater than the PRIORITY_LIMITER raise an interrupt to the CPU Special case: PRIORITY_LIMITER = 15 No interrupts can be raised to the CPU via the CPUINT, only CPUNMI can be generated.
Offset 0x03 E004			***PIC_INT_SRC***	
31:12	R/W	0	INT_TABLE_ADDR	Base address for Interrupt Handlers address table. Interrupt Handler routines address table is 4096 byte-aligned in memory.
11:3	R	0	INT_SRC	Interrupt Source identifies the highest priority pending interrupt at the time this register is read. Allows room for 511 interrupt sources. Value 0 indicates no pending interrupt.
2:0		-	Unused	Read as zero
Offset 0x03 E008—E010			***Reserved***	
Offset 0x03 E014			***PIC_INT_REG_1***	

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PRIORITY INTERRUPT CONTROLLER (M-PIC) REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
31	R	NI	INT_PENDING	Interrupt Pending Reads to this register indicate whether the interrupt is pending for service regardless of the INT_PRIORITY value and the priority limiter. 0 = intreq[i] is not asserted and INT_SET bit is not set 1 = intreq[i] is asserted or INT_SET bit is set
30	W	0	INT_SET	Interrupt Set. Writes to this register have the following effect: 0 = No effect 1 = Makes INT_PENDING =1 and INT_PRIORITY is not updated Reads return zero. Reset: INT_SET is inactive after reset.
29	W	0	INT_CLR	Interrupt Clear. Writes to this register have the following effect: 0 = No effect 1 = Makes INT_PENDING = 0 if intreq[i] is not asserted and INT_PRIORITY is not updated Reads return zero. Reset: INT_CLR is inactive after reset.
28:8		-	Unused	Read as zero
7:4	R	0	Reserved	May be used for future increase in the number of priority levels.
3:0	R/W	0	INT_PRIORITY	The INT_PRIORITY field determines the priority level of the intreq[i] line. This field is only written if INT_SET and INT_CLR are 0.

Offset 0x03 E018 ***PIC_INT_REG_2***

Interrupt register 2. This register is identical to PIC_INT_REG_1 (0x03 E014).

Offset 0x03 E01C ***PIC_INT_REG_3***

Interrupt register 3. This register is identical to PIC_INT_REG_1 (0x03 E014).

Offset 0x03 E020 ***PIC_INT_REG_4***

Interrupt register 4. This register is identical to PIC_INT_REG_1 (0x03 E014).

Offset 0x03 E024 ***PIC_INT_REG_5***

USB Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).

Offset 0x03 E028 ***PIC_INT_REG_6***

General Purpose IO Interrupt FIFO 0. This register is identical to PIC_INT_REG_1 (0x03 E014).

Offset 0x03 E02C ***PIC_INT_REG_7***

General Purpose IO Interrupt FIFO 1. This register is identical to PIC_INT_REG_1 (0x03 E014).

Offset 0x03 E030 ***PIC_INT_REG_8***

General Purpose IO Interrupt FIFO 2. This register is identical to PIC_INT_REG_1 (0x03 E014).

Offset 0x03 E034 ***PIC_INT_REG_9***

General Purpose IO Interrupt FIFO 3. This register is identical to PIC_INT_REG_1 (0x03 E014).

Offset 0x03 E038 ***PIC_INT_REG_10***

General Purpose IO Interrupt TSU. This register is identical to PIC_INT_REG_1 (0x03 E014).

Offset 0x03 E03C ***PIC_INT_REG_11***

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PRIORITY INTERRUPT CONTROLLER (M-PIC) REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
General Purpose IO TM-VIC Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E040			***PIC_INT_REG_12***	
1394 FireWire□□□□□□□□™ Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E044			***PIC_INT_REG_13***	
AICP 1 Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E048			***PIC_INT_REG_14***	
AICP 2 Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E04C			***PIC_INT_REG_15***	
I^2C 1 Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E050			***PIC_INT_REG_16***	
I^2C 2 Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E054			***PIC_INT_REG_17***	
Smartcard 1 Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E058			***PIC_INT_REG_18***	
Smartcard 2 Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E05C			***PIC_INT_REG_19***	
UART 1 Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E060			***PIC_INT_REG_20***	
UART 2 Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E064			***PIC_INT_REG_21***	
UART 3 Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E068			***PIC_INT_REG_22***	
PCI Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E06C			***PIC_INT_REG_23***	
T-PI Bus controller error Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E070			***PIC_INT_REG_24***	
M-PI Bus controller error Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E074			***PIC_INT_REG_25***	
F-PI Bus controller error Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E078			***PIC_INT_REG_26***	
2D Drawing Engine Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E07C			***PIC_INT_REG_27***	
MBS Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E080			***PIC_INT_REG_28***	
MPEG Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E084			***PIC_INT_REG_29***	
VIP 1 Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				

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PRIORITY INTERRUPT CONTROLLER (M-PIC) REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x03 E088			***PIC_INT_REG_30***	
VIP 2 Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E08C			***PIC_INT_REG_31***	
SPDIF Input Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E090			***PIC_INT_REG_32***	
SPDIF Output Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E094			***PIC_INT_REG_33***	
Audio Input 1 Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E098			***PIC_INT_REG_34***	
Audio Output 1 Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E09C			***PIC_INT_REG_35***	
Audio Input 2 Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E0A0			***PIC_INT_REG_36***	
Audio Output 2 Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E0A4			***PIC_INT_REG_37***	
Audio Input & Output 3 Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E0A8			***PIC_INT_REG_38***	
SSI Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E0AC			***PIC_INT_REG_39***	
MSP 1 MIPS Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E0B0			***PIC_INT_REG_40***	
MSP 1 TriMedia Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E0B4			***PIC_INT_REG_41***	
MSP 2 MIPS Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E0B8			***PIC_INT_REG_42***	
MSP 2 TriMedia Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E0BC			***PIC_INT_REG_43***	
Transport Stream DMA Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E0C0			***PIC_INT_REG_44***	
DMA Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E0C4			***PIC_INT_REG_45***	
Unused.				
Offset 0x03 E0C8			***PIC_INT_REG_46***	
TriMedia debug interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E0CC			***PIC_INT_REG_47***	
PCI INTA interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E0D0			***PIC_INT_REG_48***	

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PRIORITY INTERRUPT CONTROLLER (M-PIC) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Clocks module interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E0D4			***PIC_INT_REG_49***	
MSP 3 MIPS Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E0D8			***PIC_INT_REG_50***	
MSP 3 TriMedia Interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x03 E0DC—EFF0 Reserved				
Offset 0x03 EFF4			***PIC_POWERDOWN***	
31	R/W	0	POWER_DOWN	Powerdown register for the module 0 = Normal operation of the peripheral. This is the reset value. 1 = Module is powered down and module clock can be removed. At powerdown, module responds to all reads with DEADABBA (except for reads of powerdown bit) and all writes with ERR ACK (except for writes to powerdown bit).
30:0		-	Unused	Ignore during writes and read as zeroes.
Offset 0x03 EFF8			***Reserved***	
Offset 0x03 EFFC			***PIC_MOD_ ID***	
31:16	R	0x011D	MODULE ID	The PIC module ID is 0x011D.
15:12	R	1	MAJREV	Major Revision
11:8	R	0	MINREV	Minor Revision
7:0	R	0	MODULE APERTURE SIZE	Aperture size = 4kB*(bit_value+1)

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F-PI Bus Controller Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.35)

F-PI BUS CONTROLLER (FPBC) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x03 F000			***FPBC_CTRL***	
31:5		-	Unused	Ignore upon read. Write as zeroes.
4:1	R/W	0x0	TOUT_SEL[3:0]	Timeout select 0x0 = Timeout generated after 1 wait cycle. 0x1 = Timeout generated after 3 consecutive wait cycles. 0x2 = Timeout generated after 7 consecutive wait cycles. 0x3 = Timeout generated after 15 consecutive wait cycles. 0x4 = Timeout generated after 31 consecutive wait cycles. 0x5 = Timeout generated after 63 consecutive wait cycles. 0x6 = Timeout generated after 127 consecutive wait cycles. 0x7 = Timeout generated after 255 consecutive wait cycles. 0x8 = Timeout generated after 511 consecutive wait cycles. 0x9 = Timeout generated after 1,023 consecutive wait cycles. 0xa = Timeout generated after 2,047 consecutive wait cycles. 0xb = Timeout generated after 4,095 consecutive wait cycles. 0xc = Timeout generated after 8,191 consecutive wait cycles. 0xd = Timeout generated after 16,383 consecutive wait cycles. 0xe = Timeout generated after 32,767 consecutive wait cycles. 0xf = Timeout generated after 65,535 consecutive wait cycles.
0	R/W	0x1	TOUT_OFF	Timeout disable 0x0 = Timeout enabled. 0x1 = Timeout disabled.
Offset 0x03 F00C			***FPBC_ADDR***	
31:2	R	0x0000 0000-	ERR_TOUT_ADDR[31:2]	Full 30 bits of the F-PI address bus which causes a PI error or timeout.
1:0		-	Unused	Ignore upon read. Write as zeroes.
Offset 0x03 F010			***FPBC_STAT***	
31:27		-	Unused	Ignore upon read. Write as zeroes.
26:24	R	0x0	ERR_TOUT_GNT[2:0]	Active master causing error or timeout 0x1 = EJTAG 0x2 = MIPS side of M-bridge 0x4 = MIPS processor.
23:20		-	Unused	Ignore upon read. Write as zeroes.

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F-PI BUS CONTROLLER (FPBC) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
19:16	R	0x0	ERR_TOUT_SEL[3:0]	Selected agent during error or timeout 00 = MIPS PIC or None 01 = Fast PI to Memory highway bus Interface (F-PIMI) 02 = MIPS side of M-bridge 03 = F-PI Bus controller 04 = MIPS processor debug (DSU) 05 = EJTAG 1MB probe memory 06 = EJTAG data registers 07 = MIPS exception handling space 08 = Null 09 = Default slave. **Note:** MIPS PIC is not specifically identified.
15:13		-	Unused	Ignore upon read. Write as zeroes.
12:8	R	0x00	ERR_TOUT_OPC[4:0]	Opcode causing an error or timeout 0x00 = No-operation (no communication with bus slave agent) 0x01 = Block of 32 words, regular address space 0x02 = 1 word, regular address space 0x03 = 1 word, control address space 0x04 = Block of 2 words, regular address space 0x05 = Block of 4 words, regular address space 0x06 = Block of 8 words, regular address space 0x07 = Block of 16 words, regular address space 0x08 = 1 half word address [1:0] = 00, regular address space 0x09 = 1 triple-byte address [1:0] = 00, regular address space 0x0a = 1 halfword address [1:0] = 10, regular address space 0x0b = 1 triple-byte address [1:0] = 01, regular address space 0x0c = 1 byte address [1:0] = 00, regular address space 0x0d = 1 byte address [1:0] = 01, regular address space 0x0e = 1 byte address [1:0] = 10, regular address space 0x0f = 1 byte address [1:0] = 11, regular address space 0x10 = Reserved 0x11 = Reserved 0x12 = 1 double word, regular address space 0x13 = Reserved 0x14 = block of 2 double words, regular address space 0x15 = block of 4 double words, regular address space 0x16 = block of 8 double words, regular address space 0x17 = block of 16 double words, regular address space The rest are reserved.
7:3		-	Unused	Ignore upon read. Write as zeroes.

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F-PI BUS CONTROLLER (FPBC) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
2:0	R	0x0	ERR_TOUT_ACK[2:0]	Acknowledge during error or timeout 0x0 = Wait: bus operation not completed in current bus cycle. 0x1 = Ready-More: bus operation successfully completed in current bus cycle and slave is immediately able to process a further bus operation of the same data direction. 0x2 = Error: bus operation has lead to error condition 0x3 = Ready: bus operation, successfully completed in current bus cycle. 0x4 = Retract: refuse to complete bus operation. The rest are reserved.
Offset 0x03 F014			***FPBC_MON***	
31:19		-	Unused	Ignore upon read. Write as zeroes.
18:16	R	0x0	GNT_LAST[2:0]	Last active master 0x1 = EJTAG 0x2 = MIPS side of M-bridge 0x4 = MIPS processor.
15:3		-	Unused	Ignore upon read. Write as zeroes.
2:0	R	0x0	REQ_CURR[2:0]	Current requests 0x1 = EJTAG 0x2 = MIPS side of M-bridge 0x4 = MIPS processor.
Offset 0x03 F018			***EN_EJT_DSU_APERTURE***	
31:1		-	Unused	Ignore upon read. Write as zeroes.
0	R/W	0x1	EN_EJT_DSU_APERTURE	Enable EJTAG probe memory and MIPS DSU spaces 0 = PI addresses from FF20_0000 to FF2F_FFFFdo not generate an EJTAG probe memory. PI select and PI addresses from FF30_0000 to FF3F_FFFF don't generate a MIPS DSU PI select. 1 = PI addresses from FF20_0000 to FF2F_FFFFgenerate an EJTAG probe memory. PI select and PI addresses from FF30_0000 to FF3F_FFFF generate a MIPS DSU PI select.
Offset 0x03 F01C			***EN_MIPS_EXT_WBEMPTY***	
31:1		-	Unused	Ignore upon read. Write as zeroes.
0	R/W	0x1	EN_MIPS_EXT_WBEMPTY	Enable signal to tell MIPS that its external buffer is full 0 = MIPS external write buffer empty signal is kept always high. Used when the MIPS external write buffer (F-PIMI) is programmed to non-posted writes. 1 = MIPS external write buffer empty signal equals the inverted version of F-PIMI busy. Used when the MIPS external write buffer F-PIMI is programmed to posted writes.

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F-PI BUS CONTROLLER (FPBC) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x03 F020			***MIPS_BOOT_ADR0***	
31:0	R/W	0x3c08 a010	MIPS_BOOT_ADR0[31:0]	Exception handling register for Boot. This register usually contains a load register command. It is used to get the MIPS to load the jump address into a MIPS register. The reset value of this register = lui t0,0xA0F0 which means load the jump address A0F0_0000 into MIPS register t0. A010_0000 is 1Mbyte above zero uncached kernel mode.
Offset 0x03 F024			***MIPS_BOOT_ADR4***	
31:0	R/W	0x0100 0008	MIPS_BOOT_ADR4[31:0]	Exception handling register for Boot. This register usually contains a jump register command. It is used to get the MIPS to jump to the address that is stored in a MIPS register. The reset value of this register = jr t0 which means jump to the address stored in MIPS register t0.
Offset 0x03 F028			***MIPS_BOOT_ADR8***	
31:0	R/W	0x0000 0000	MIPS_BOOT_ADR8[31:0]	Exception handling register for Boot. This register usually contains a NOP command. It is used to get the MIPS to do No Operation. Reset value = NOP.
Offset 0x03 F02C			***MIPS_BOOT_ADRC***	
31:0	R/W	0x0000 0000	MIPS_BOOT_ADRC[31:0]	Exception handling register for Boot. This register usually contains a NOP command. It is used to get the MIPS to do No Operation. Reset value = NOP.
Offset 0x03 F034			***EN_MIPS_REMAP_FPBC***	
31:1		-	Unused	Ignore upon read. Write as zeroes.
0	R/W	0x1	EN_MIPS_REMAP_FPBC	Enables remapping of MIPS exception handling addresses to F-PI Bus controller registers. 0 = Do not remap MIPS exception handling addresses. 1 = Remap MIPS exception handling addresses to F-PI Bus controller registers.
Offset 0x03 F040			***SW_EXC_ADR0***	
31:0	R/W	0x3c08 a020	SW_EXC_ADR0[31:0]	Exception handling register for software debug. This register usually contains a load register command. It is used to get the MIPS to load the jump address into a MIPS register. The reset value of this register = lui t0,0xA020 which means load the jump address A020_0000 into MIPS register t0. A020_0000 is 2 MB above zero uncached kernel mode.
Offset 0x03 F044			***SW_EXC_ADR4***	
31:0	R/W	0x0100 0008	SW_EXC_ADR4[31:0]	Exception handling register for Boot. This register usually contains a jump register command. It is used to get the MIPS to jump to the address that is stored in a MIPS register. The reset value of this register = jr t0 which means jump to the address stored in MIPS register t0.

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F-PI BUS CONTROLLER (FPBC) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x03 F048			***SW_EXC_ADR8***	
31:0	R/W	0x0000 0000	SW_EXC_ADR8[31:0]	Exception handling register for Boot. This register usually contains a NOP command. It is used to get the MIPS to do No Operation. Reset value = NOP.
Offset 0x03 F04C			***SW_EXC_ADRC***	
31:0	R/W	0x0000 0000	SW_EXC_ADRC[31:0]	Exception handling register for Boot. This register usually contains a NOP command. It is used to get the MIPS to do No Operation. Reset value = NOP.
Offset 0x03 FFE0			***FPBC_INT_STATUS***	
31:2		-	Unused	Ignore upon read. Write as zeroes.
1	R	0	INT_STATUS_TOUT	Timeout interrupt status register. It reports any pending timeout interrupts: 1 = Timeout interrupt pending, meaning F-PI Bus controller has generated a timeout because some F-PI device has violated the programmable limit for timeout (see FPBC_TOUT) or M-bridge generated a timeout request (see PI-PI bridge). 0 = Timeout interrupt not pending.
0	R	0	INT_STATUS_ERROR	Error interrupt status register. It reports any pending error interrupts 1 = Error interrupt pending. F-PI Bus controller has detected an error acknowledge on the F-PI Bus. 0 = Error interrupt not pending.
Offset 0x03 FFE4			***FPBC_INT_EN***	
31:2		-	Unused	Ignore upon read. Write as zeroes.
1	R/W	0	INT_ENABLE_TOUT	Timeout interrupt enable register 1 = Timeout interrupt is enabled. 0 = Timeout interrupt is disabled.
0	R/W	0	INT_ENABLE_ERROR	Timeout interrupt enable register 1 = Error interrupt is enabled 0 = Error interrupt is disabled.
Offset 0x03 FFE8			***FPBC_INT_CLR***	
31:2		-	Unused	Ignore upon read. Write as zeroes.
1	W	0	INT_CLEAR_TOUT	Timeout interrupt clear register. This is written by software to clear the interrupt. 1 = Timeout interrupt is cleared. 0 = Timeout interrupt is not cleared.
0	W	0	INT_CLEAR_ERROR	Error interrupt clear register. This is written by software to clear the interrupt. 1 = Error interrupt is cleared. 0 = Error interrupt is not cleared.

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F-PI BUS CONTROLLER (FPBC) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x03 FFEC			***FPBC_INT_SET***	
31:2		-	Unused	Ignore upon read. Write as zeroes.
1	W	0	INT_SET_TOUT	Timeout interrupt set register. Allows software to set interrupts. 1 = Timeout interrupt is set. 0 = Timeout interrupt is not set.
0	W	0	INT_SET_ERROR	Error interrupt set register. Allows software to set interrupts. 1 = Error interrupt is set. 0 = Error interrupt is not set.
Offset 0x03 FFF0—FFF8			***Reserved***	
Offset 0x03 FFFC			***FPBC_MODULE_ID***	
31:16	R	0x0102	MODULE_ID[15:0]	Unique 16-bit code. Module ID 0 and 1 are reserved for future use. Value 0x0102 is for the PNX8526 F-PI Bus controller module.
15:12	R	0	MAJREV[3:0]	Major Revision: any revision that might break software compatibility.
11:8	R	1	MINREV[3:0]	Minor Revision: any revision that keeps software compatible.
7:0	R	0	MODULE_APERTURE_SIZE	Aperture size = 4 kB*(bit_value+1), so 0 means 4 kB (the default).

PCI-XIO Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.35)

PCI-XIO REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
PCI Control Registers				
Offset 0x04 0000			***PCI Interrupt Status***	
31:21	R	0	Reserved	
20	R	0	pwrstate_chg	Power management register has been changed.
19	R	0	xio_acc_err	XIO access error. XIO or PCI master not enabled.
18	R	0	pim_rd_err	PI master read error detected.
17	R	0	pim_wr_err	PI master write error detected.
16	R	0	pis_rd_err	PI slave read error detected.
15	R	0	pis_wr_err	PI slave write error detected.
14	R	0	xio_ack_done	Rising edge of xio_ack has been observed.
13	R	0	gpxio_done	GPXIO transaction completed.
12	R	0	dma_done	DMA transaction completed.
11	R	0	serr_seen	SERR observed on PCI bus.

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PCI-XIO REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
10	R	0	gppm_done	General purpose PCI command completed.
9	R	0	err_bad_cmd	Non-supported DMA command attempted or other error.
8	R	0	err_base10_subword	Subword attempt to base10 aperture when restrained to word only (not used on the PNX8526).
7	R	0	err_base14_subword	Subword attempt to base14 aperture when restrained to word only.
6	R	0	err_base18_subword	Subword attempt to base18 aperture when restrained to word only (not used on the PNX8526).
5	R	0	mstr_parity err	PCI master set or observed parity error (PERR).
4	R	0	err_parity	Detected parity error (PERR).
3	R	0	err_sys	Signaled system error (SERR)
2	R	0	err_r_mabort	Received Master Abort.
1	R	0	err_r_tabor	Received Target Abort.
0	R	0	err_s_tabort	Signaled Target Abort.
Offset 0x04 0004			***PCI Interrupt Enable***	
31:21	R	0	Reserved	
20	R/W	0	en_int_pwrstate_chg	Enable interrupt on change of power state register.
19	R/W	0	en_int_xio_acc_err	Enable interrupt on XIO access error.
18	R/W	0	en_int_pim_rd_err	Enable interrupt on PI master read error.
17	R/W	0	en_int_pim_wr_err	Enable interrupt on PI master write error.
16	R/W	0	en_int_pis_rd_err	Enable interrupt on PI slave read error.
15	R/W	0	en_int_pis_wr_err	Enable interrupt on PI slave write error.
14	R/W	0	en_int_xio_ack_done	Enable interrupt on rising edge of xio_ack done.
13	R/W	0	en_int_gpxio_done	Enable interrupt on gpxio_done.
12	R/W	0	en_int_dma_done	Enable interrupt on dma_done.
11	R/W	0	en_int_serr_seen	Enable interrupt on SERR observed on PCI bus.
10	R/W	0	en_int_gppm_done	Enable interrupt on general purpose PCI master cycle done.
9	R/W	0	en_int_bad_cmd	Enable interrupt on Bad-Command status.
8	R/W	0	en_int_base10_subword	Enable interrupt on subword attempt to Base10 error status.
7	R/W	0	en_int_base14_subword	Enable interrupt on subword attempt to Base14 error status.
6	R/W	0	en_int_base18_subword	Enable interrupt on subword attempt to Base18 error status.
5	R/W	0	en_int_mstr_parity err	Enable interrupt on Master Parity Error.
4	R/W	0	en_int_parity	Enable interrupt on Parity Error status.
3	R/W	0	en_int_err_sys	Enable interrupt on System Error status.
2	R/W	0	en_int_r_mabort	Enable interrupt on received Master Abort status.
1	R/W	0	en_int_r_tabort	Enable interrupt on received Target Abort status.
0	R/W	0	en_int_s_tabort	Enable interrupt on signaled Target Abort status.

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PCI-XIO REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x04 0008			*PCI Interrupt Clear*	
31:21	R	0	Reserved	
20	W	0	clr_pwrstate_chg	Clear power state change register flag.
19	W	0	clr_xio_acc_err	Clear XIO access error.
18	W	0	clr_pim_rd_err	Clear PI master read error flag.
17	W	0	clr_pim_wr_err	Clear PI master write error flag.
16	W	0	clr_pis_rd_err	Clear PI slave read error flag.
15	W	0	clr_pis_wr_err	Clear PI slave write error flag.
14	W	0	clr_xio_ack_done	Clear xio_ack done flag.
13	W	0	clr_gpxio_done	Clear GPXIO done flag.
12	W	0	clr_dma_done	Clear dma_done flag.
11	W	0	clr_serr_seen	Clear serr_seen flag.
10	W	0	clr_gppm_done	Clear GPPM done flag.
9	W	0	clr_bad_cmd	Clear Bad-Command status.
8	W	0	clr_base10_subword	Clear subword attempt to Base10 error status.
7	W	0	clr_base14_subword	Clear subword attempt to Base14 error status.
6	W	0	clr_base18_subword	Clear subword attempt to Base18 error status.
5	W	0	clr_mstr_parity err	Clear Master Parity Error.
4	W	0	clr_parity	Clear Parity Error status.
3	W	0	clr_err_sys	Clear System Error status.
2	W	0	clr_r_mabort	Clear received Master Abort status.
1	W	0	clr_r_tabort	Clear received Target Abort status.
0	W	0	clr_s_tabort	Clear signaled Target Abort status.
Offset 0x04 000C			*PCI Interrupt Set*	
31:21	R	0	Reserved	
20	W	0	set_pwrstate_chg	Set change of power state register flag.
19	W	0	set_xio_acc_err	Set XIO access error.
18	W	0	set_pim_rd_err	Set PI master read error flag.
17	W	0	set_pim_wr_err	Set PI master write error flag.
16	W	0	set_pis_rd_err	Set PI slave read error flag.
15	W	0	set_pis_wr_err	Set PI slave write error flag.
14	W	0	set_xio_ack_done	Set xio_ack done flag.
13	W	0	set_gpxio_done	Set GPXIO done flag.
12	W	0	set_dma_done	Set dma_done flag.
11	W	0	set_serr_seer	Set serr_seen flag.
10	W	0	set_gppm_done	Set gppm_done flag.

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PCI-XIO REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
9	W	0	set_bad_cmd	Set Bad-Command status.
8	W	0	set_base10_subword	Set subword attempt to Base10 error status.
7	W	0	set_base14_subword	Set subword attempt to Base14 error status.
6	W	0	set_base18_subword	Set subword attempt to Base18 error status.
5	W	0	set_mstr_parity err	Set master Parity Error.
4	W	0	set_parity	Set Parity Error status.
3	W	0	set_err_sys	Set System Error status.
2	W	0	set_r_mabort	Set received Master Abort status.
1	W	0	set_r_tabort	Set received Target Abort status.
0	W	0	set_s_tabort	Set signaled Target Abort status.
Offset 0x04 0010			***PCI Setup***	
This register must be initialized before any PCI cycles will be entertained. The boot loader is expected to load the values at boot time. Write once by boot loader, otherwise read only. Because this register is “written once” the bit fields are designated “R/W1.”				
31:28	R	0	Reserved	
27	R/W1	1	d2_support	Support for D2 power state
26	R/W1	1	d1_support	Support for D1 power state
25	R/W1	0	Reserved	
24	R/W1	0	en_ta	Terminate restricted access attempt with target abort (otherwise, ignore writes, return 0 on read).
23	R/W1	0	en_pci2mmi	Enable memory hwy interface.
22	R/W1	0	en_xio	Enable XIO functionality.
21	R/W1	0	base18_prefetchable	PCI base address 18 is a prefetchable memory aperture.
20:18	R/W1	011	base18_siz	The size of aperture located by PCI cfg base 18 is: 011 = 16 MB 100 = 32 MB 101 = 64 MB 110 = 128 MB This aperture is used as the XIO aperture in the PNX8526.
17	R/W1	1	en_base18	Enable 3rd aperture, PCI base address 18 (non-PNX8526 application). The PNX8526 will always use this aperture.
16	R/W1	0	base14_prefetchable	PCI Base address 14 is a prefetchable memory aperture.
15	R	0	Reserved	
14:12	R/W1	000	base14_siz	The size of aperture located by PCI cfg base 14 is: 000 = 2 MB or 32 if IO This aperture is used as the MMIO aperture in the PNX8526.
11	R/W1	1	en_base14	Enable 2nd aperture, PCI base address 14 (non-PNX8526 application). The PNX8526 will always use this aperture.
10	R/W1	1	base10_prefetchable	PCI Base address 10 is a prefetchable memory aperture.

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PCI-XIO REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
9:7	R/W1	100	base10_siz	The size of aperture located by PCI cfg base 10 is: 011 = 16 MB 100 = 32 MB 101 = 64 MB This aperture is used as the DRAM aperture in the PNX8526.
6:2			Reserved	
1	R/W1	0	en_config_manag	Enable configuration management.
0	R/W1	0	en_pci_arb	Enable PCI system arbitration.
Offset 0x04 0014			***PCI Control***	
31:10	R	0	Reserved	
9	R/W	0	en_serr_seen	Enable monitoring of the SERR pin.
8	R/W	0	en_pi_wp	Enable write-posting from PI-Bus.
7	R/W	0	en_wrlock	Enables locked PI-write transactions originating from PCI. If this bit is '0' the bridge breaks down a burst from the PCI side into single WDU writes on the PI side.
6	R/W	0	en_base10_spec_rd	Read ahead to optimize PCI read latency to base 10.
5	R/W	0	en_base14_spec_rd	Read ahead to optimize PCI read latency to base 14.
4	R/W	0	en_base18_spec_rd	Read ahead to optimize PCI read latency to base 18.
3	R/W	0	disable_subword2_10	Disable subword access to/from Base10 aperture.
2	R/W	1	disable_subword2_14	Disable subword access to/from Base14 aperture.
1	R/W	1	disable_subword2_18	Disable subword access to/from Base18 aperture.
0	R/W	1	en_retry_timer	Enables timer for 16 tic rule enforcer. This bit does not affect access to the XIO aperture.
Offset 0x04 0018			***PCI_Base1_lo***	
31:21	R/W	0	pci_base1_lo	For internal address decoding: low bar of first aperture for external PCI access. This register affects the decode and routing of the bus controllers. It should not be relied on as stable for 10 clocks after writing. It is recommended that the PCI_Base1_lo be initialized before the PCI_Base1_hi to avoid a potentially large segment of address space being temporarily allocated to PCI space.
20:0	R	0	Reserved	
Offset 0x04 001C			***PCI_Base1_hi***	
31:21	R/W	0	pci_base1_hi	For internal address decoding: high bar of first aperture for external PCI access (up to but not including). This register affects the decode and routing of the bus controllers. It should not be relied on as stable for 10 clocks after writing. It is recommended the PCI_Base1_lo be initialized before the PCI_Base1_hi to avoid a potentially large segment of address space being temporarily allocated to PCI space.
20:0	R	0	Reserved	

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PCI-XIO REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x04 0020			***PCI_Base2_lo***	
31:21	R/W	0	pci_base2_lo	For internal address decoding: low bar of second aperture for external PCI access. This register affects the decode and routing of the bus controllers. It should not be relied on as stable for 10 clocks after writing. It is recommended the PCI_Base2_lo be initialized before the PCI_Base2_hi to avoid a potentially large segment of address space being temporarily allocated to PCI space.
20:0	R	0	Reserved	
Offset 0x04 0024			***PCI_Base2_hi***	
31:21	R/W	0	pci_base2_hi	For internal address decoding: high bar of second aperture for external PCI access (up to but not including). This register affects the decode and routing of the bus controllers. It should not be relied on as stable for 10 clocks after writing. It is recommended the PCI_Base2_lo be initialized before the PCI_Base2_hi to avoid a potentially large segment of address space being temporarily allocated to PCI space.
20:0	R	0	Reserved	
Offset 0x04 0028			***Read Data Lifetime Timer***	
31:16		-	Unused	
15:0	R/W	8000	read_lifetime	This register is the amount of time (in PCI clocks) that the PCI will hold a piece of data exclusively for an external PCI master. The timer is initiated when the PCI can not complete the requested read in 16 clock cycles and issues a retry.
Offset 0x04 002C			***General Purpose PCI Master (GPPM) Address***	
31:0	R/W	0	gppm_addr	This register will be written with the address for the single data phase cycle to be issued on the PCI bus. It will accept only 32-bit writes. When issuing type 0 configuration transactions, the device number (bits [15:11]) is expanded to bits [31:11] on the PCI bus.
Offset 0x04 0030			***General Purpose PCI Master (GPPM) Write Data***	
31:0	R/W	0	gppm_wdata	This register will be written with the data for the single data phase cycle to be issued on the PCI bus. This register will accept any size write.
Offset 0x04 0034			***General Purpose PCI Master (GPPM) Read Data***	
31:0	R	0	gppm_rdata	This register will hold data from the selected target after completion of the read.
Offset 0x04 0038			***General Purpose PCI Master (GPPM) Control***	
31:11	R	0	Reserved	
10	R	0	gppm_done	1 = cycle has completed. This bit can also be viewed in the pci_status register. Write to register 0008 to clear.
9	R/W	0	init_pci_cycle	1 = initiate a PCI single data phase transaction on the PCI bus with address “gppm_addr” and data “gppm_data.”
8	R	0	Reserved	

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PCI-XIO REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
7:4	R/W	0	gppm_cmd	Command to be used with PCI cycle. The acceptable commands to use in the command field include IO read, IO write, memory Read, memory Write, configuration read and interrupt acknowledge. If configuration management is enabled, configuration write may be used.
3:0	R/W	0	gppm_ben	Byte enables to be used with PCI cycle
Offset 0x04 0040			***Image of Device ID and Vendor ID***	
31:16	R	0x8500	device_id	PCI configuration device ID
15:0	R	0x1131	vendor_id	PCI configuration vendor ID
Offset 0x04 0044			***Image of Command/Status***	
31:16	R	0x0290	status	PCI configuration status register
15:0	R/W*	0x0000	command	PCI configuration command register. *This register is read/write if configuration management is enabled (pci_setup[1]). If not enabled, it is read only. Refer to configuration register 4 for details on which bit are implemented and are controllable.
Offset 0x04 0048			***Image of Class Code/Revision ID***	
31:8	R/W1*	040000	class code	PCI configuration class code. *Write-once/Read-only
7:0	R	0	revision id	PCI configuration revision ID
Offset 0x04 004C			***Image of Latency Timer/Cache Line Size***	
31:24	R	0	BIST	PCI configuration BIST
23:16	R	0	Header Type	PCI configuration Header Type
15:8	R/W*	0	latency timer	PCI configuration latency timer. *This register is read/write if configuration management is enabled (pci_setup[1]). If not enabled, it is read only.
7:0	R/W*	0	cache line size	PCI configuration cache line size. *This register is read/write if configuration management is enabled (pci_setup[1]). If not enabled, it is read only.
Offset 0x04 0050			***Base Address 10 Image***	
31:4	R/W*	0	Base Address 10	PCI configuration Base address for DRAM. This register affects the decode and routing of the bus controllers. It should not be relied on as stable for 10 clocks after writing. *This register is read/write if configuration management is enabled (pci_setup[1]). If not enabled, it is read only.
3	R	cfg	Prefetchable	Value is determined at boot time.
2:0	R	0	Type	Indicates type 0 memory space (locatable anywhere in 32-bit address space).

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PCI-XIO REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x04 0054			***Base Address 14 Image***	
31:4	R/W*	0	Base Address 14	PCI configuration Base address for MMIO. This register affects the decode and routing of the bus controllers. It should not be relied on as stable for 10 clocks after writing. *This register is read/write if configuration management is enabled (pci_setup[1]). If not enabled, it is read only.
3	R	cfg*	Prefetchable	Value is determined at boot time. *Value determined by PCI Setup register.
2:0	R	0	Type	Indicates type 0 memory space (locatable anywhere in 32-bit address space).
Offset 0x04 0058			***Base Address 18 Image***	
31:4	R/W*	0	Base Address 18	PCI configuration Base address for XIO. This register affects the decode and routing of the bus controllers. It should not be relied on as stable for 10 clocks after writing. This register is read/write if configuration management is enabled (pci_setup[1]). If not enabled, it is read only.
3	R	cfg	Prefetchable	Value is determined at boot time.
2:0	R	0	Type	Indicates PCI “type 0” memory space (locatable anywhere in 32-bit address space).
Offset 0x04 006C			***Subsystem ID/Subsystem Vendor ID Write Port***	
This register must be initialized before any PCI cycles will be entertained. The boot loader is expected to load the values at boot time. This register is a Write-once/Read-only register (R/W1).				
31:16	R/W1	0	subsystem ID	This is the write port for the Subsystem ID (PCI config 2C).
15:0	R/W1	0	subsystem vendor ID	This is the write port for the Subsystem Vendor ID (PCI config 2C).
Offset 0x04 0070			***Reserved***	
Offset 0x04 0074			***Image of Configuration Reg 34***	
31:8	R	0	Reserved	
7:0	R	40	CAP_PTR	Capabilities Pointer
Offset 0x04 007C			***Image of Configuration Reg 3C***	
31:24	R	0x18	max_lat	Max Latency
23:16	R	0x09	min_gnt	Minimum Grant
15:8	R	0x01	interrupt pin	Interrupt pin information
7:0	R/W*	0x00	Interrupt Line	This register conveys interrupt line routing information. *This register is read/write if configuration management is enabled (pci_setup[1]). If not enabled, it is read only.
Offset 0x04 0080			***Image of Configuration Reg 40***	
31:27	R	00000	Reserved	
26	R	cfg*	d2_support	1 = Device supports D2 power management state. *Value determined by PCI Setup register.

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PCI-XIO REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
25	R	cfg*	d1_support	1 = Device supports D1 power management state. *Value determined by PCI Setup register.
24:19	R	0	Reserved	
18:16	R	010	version	Indicates compliance with version 1.1 of PM.
15:8	R	00	Next Item Pointer	There are no other extended capabilities.
7:0	R	01	Cap_ID	Indicates this is power management data structure.
Offset 0x04 0084			***Image of Configuration Reg 44***	
31:2	R	0	Reserved	
1:0	R/W*	0	pwr_state	Power State *This register is read/write if configuration management is enabled (pci_setup[1]). If not enabled, it is read only.
Offset 0x04 0800			***DMA PCI Address***	
This register will accept only word writes.				
31:0	R/W	1c00_0000	dma_eaddr	This is the external starting address for the DMA engine. It is used for DMA transfers over PCI and XIO. Bit 0 and 1 are not used because all DMA transfers are word aligned.
Offset 0x04 0804			***DMA Internal Address***	
This register will accept only word writes.				
31:0	R/W	0010_0000	dma_iaddr	This is the internal read source/ write destination address in SDRAM.
Offset 0x04 0808			***DMA Transfer Size***	
This register will accept any size writes.				
31:16	R/W	0	Reserved	
15:0	R/W	800	dma_length	This is the length of the DMA transfer (number of 4-byte words).
Offset 0x04 080C			***DMA Controls***	
This register will accept any size writes.				
31:10	R	0	Reserved	
9	R/W	0	snd2xio	0 = DMA will target PCI. 1 = DMA will target XIO.
8	R/W	0	fix_addr	0 = DMA will use linear address. 1 = DMA will use a fixed address (for XIO).
7:5	R/W	0	max_burst_size	PCI transaction will be split into multiple transactions. Max size: 000 = 8 data phase 001 = 16 data phase 010 = 32 data phase 011 = 64 data phase 100 = 128 data phase 101 = 256 data phase 110 = 512 data phase 111 = No restriction in transfer length

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PCI-XIO REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
4	R/W	0	init_dma	Initiate DMA transaction. This bit is cleared by the DMA engine when it begins its operation.
3:0	R/W	0	cmd_type	Command to be used for DMA. This field is restricted to memory type commands.
Offset 0x04 0810			***XIO Control Register***	
31:2	R	0	Reserved	
1	R		xio_ack	Live XIO_ACK status bit.
0	R/W	0	Reserved	
Offset 0x04 0814			***XIO Sel0 Profile***	
This register sets up the profile of the XIO select 0 line. All times are in reference to PCI clocks.				
31:23	R	0	Reserved	
22	R/W	0	sel0_use_ack	0 = Fixed wait state 1 = Wait for ACK Not used for IDE.
21:18	R/W	0	sel0_we_hi	68360: DS time high. NOR: WN time high NAND: REN profile, [19:18] low time; [21:20] high time IDE: DIOR and DIOW high time
17:14	R/W	0	sel0_we_lo	68360: Not used. NOR: WN time low NAND: WEN profile, [15:14] low time; [17:16] high time IDE: DIOR and DIOW low time
13:9	R/W	0	sel0_wait	68360: DS time low if using fixed timing. NOR: OEN time low if not using ACK. NAND: Delay between address and data phase if not using ACK, delay until monitoring ACK. IDE: Not used.
8:5	R/W	0	sel0_offset	Starting address offset from start address of XIO aperture, in 8M increments. This field must be naturally aligned with the size of the profile.
4:3	R/W	0	sel0_type	Device type selected: 00 = 68360 type device 01 = NOR Flash 10 = NAND-Flash 11 = IDE
2:1	R/W	0	sel0_siz	Amount of address space allocated to Sel0: 00 = 8M 01 = 16M 10 = 32M 11 = 64M
0	R/W	0	en_sel0	1 = Enable sel0 profile.
Offset 0x04 0818			***XIO Sel1 Profile***	
This register sets up the profile of the XIO select 1 line. All times are in reference to PCI clocks.				
31:23	R	0	Reserved	

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PCI-XIO REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
22	R/W	0	sel1_use_ack	1 = Wait for ACK 0 = fixed wait state. Not used for IDE.
21:18	R/W	0	sel1_we_hi	63860: time high. NOR: WN time high NAND: REN profile, [19:18] low time; [21:20] high time IDE: DIOR and DIOW high time
17:14	R/W	0	sel1_we_lo	63860: Not used. NOR: WN time low NAND: WEN profile, [15:14] low time; [17:16] high time IDE: DIOR and DIOW low time
13:9	R/W	0	sel1_wait	63860: DS time low if using fixed timing. NOR: OEN time low if not using ACK. NAND: Delay between address and data phase if not using ACK, delay until monitoring ACK. IDE: Not used.
8:5	R/W	0	sel1_offset	Address offset form start address of XIO aperture, in 8M increments. This field must be naturally aligned with the size of the profile.
4:3	R/W	0	sel1_type	Sel1 is configured as: 00 = 68360 type device 01 = NOR Flash 10 = NAND-Flash 11 = IDE
2:1	R/W	0	sel1_siz	Amount of address space allocated to Sel1: 00 = 8M 01 = 16M 10 = 32M 11 = 64M
0	R/W	0	en_sel1	Enable sel1 profile.
Offset 0x04 081C			***XIO Sel2 Profile***	
This register sets up the profile of the XIO select 2 line. All times are in reference to PCI clocks.				
31:23	R	0	Reserved	
22	R/W	0	sel2_use_ack	0 = Fixed wait state. 1 = Wait for ACK Not used for IDE
21:18	R/W	0	sel2_we_hi	68360: DS time high. NOR: WN time high NAND: REN profile, [19:18] low time; [21:20] high time IDE: DIOR and DIOW high time
17:14	R/W	0	sel2_we_lo	63860: Not used. NOR: WN time low NAND: WEN profile, [15:14] low time; [17:16] high time IDE: DIOR and DIOW low time

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PCI-XIO REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
13:9	R/W	0	sel2_wait	68360: DS time low if using fixed timing. NOR: OEN time low if not using ACK. NAND: Delay between address and data phase if not using ACK, delay until monitoring ACK. IDE: Not used.
8:5	R/W	0	sel2_offset	Address offset form start address of XIO aperture, in 8M increments. This field must be naturally aligned with the size of the profile.
4:3	R/W		sel2_type	Sel2 is configured as: 00 = 68360 type device 01 = NOR Flash 10 = NAND-Flash 11 = IDE
2:1	R/W	0	sel2_siz	Amount of address space allocated to Sel2: 00 = 8M 01 = 16M 10 = 32M 11 = 64M
0	R/W	0	en_sel2	Enable sel2 profile.
Offset 0x04 0820			***GPXIO_address***	
31:0	R/W	0	gpxio_addr	General Purpose XIO cycle address. This register sets the address for an indirect read or write to/from XIO address space. Only 4 byte writes are allowed in this register. The values programmed for bits 0 and 1 are not used by the XIO module. Refer to gpxio_ben.
Offset 0x04 0824			***GPXIO_write_data***	
31:0	R/W	0	gpxio_wdata	General Purpose XIO cycle data. This register is programmed with data for a write cycle.
Offset 0x04 0828			***GPXIO_read_data***	
31:0	R	0	gpxio_rdata	General Purpose XIO cycle data. This register contains the data of a read cycle after completion.
Offset 0x04 082C			***GPXIO_ctrl***	
This register controls the type of access to XIO and provides status.				
31:11	R	0	Reserved	
10	W	0	set_gpxio_done	Set gpxio_done.
9	R	0	gpxio_cyc_pending	1 = GPXIO transaction on XIO is pending.
8	R	0	gpxio_done	General Purpose XIO cycle complete. This bit may also be set by writing 1 to bit 10 (set_gpxio_done). This bit is cleared by writing 1 to bit 6 or 7.
7	R/W	0	clr_gpxio_done	1 = Clear “gpxio_done.”
6	R/W	0	gpxio_init	1 = Initiate a transaction on XIO. The type of transaction will match the profile of the selected aperture. This bit gets cleared if the cycle has been initiated. This bit clears bit 8 if set.
5	R/W	0	gpxio_int	Generate interrupt on completion of XIO cycle.

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PCI-XIO REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
4	R/W	0	gpxio_rd	Read/not write command on XIO
3:0	R/W	0	gpxio_ben	Active low byte enables to be used on the indirect XIO cycle. These are used to determine how many bytes to access and the lower two address bits for use in “gpxio_addr”.
Offset 0x04 0830			***NAND-Flash controls***	
21:16	R/W	17	nand_ctrls	This field controls the type of NAND-Flash access cycle. The bits are defined as follows: [21]: 1 = Enable access to spare area; 0: access normal area [20]: 1 = Include data in access cycle; 0 access does not include data phase(s) [19:18] = Number of commands to be used in NAND-Flash access [17:16] = Number of address phases to be used in NAND-Flash access.
15:8	R/W	0	command_b	This is the second command for NAND-Flash when two commands are required to complete a cycle.
7:0	R/W	0	command_a	This is the command type to be used with NAND-Flash cycles when one or more commands are required to complete a cycle.
Offset 0x04 0FFC			***Module ID***	
31:16	R	0x0113	Module ID	PNX8526 Module ID
15:12	R	0	Major Revision number	Major Revision number
11:8	R	1	Minor revision number	Minor revision number
7:0	R	0	mod_size	Module size is 4 kB.

Spy Micro-Architecture Registers

(Appendix1)

SPY MICRO-ARCHITECTURE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x04 1000			***DBG_SPY_ADDR_REG***	
31	W	0	spy_enable	If 1, SPY signals are sent to the designated chip output pins
30	W	0	mips_pc_trace_enable	If 1, MIPS PC trace signals are multiplexed onto the SPY outputs
29:17	R	NI	Reserved	Read as 0.
16:0	R/W	0	spy_addr	17-bit SPY micro-architecture address
Offset 0x04 1004			***DBG_SPY_DATA_REG***	
31:12	R	NI	Reserved	Read as 0.
11:0	R	0	spy_data[11:0]	Contains the value of the 12 SPY outputs sampled on the PI-Bus clock.

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SPY MICRO-ARCHITECTURE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x04 1008			***DBG_SPY_ALIGN_REG0***	
31:28	R/W	0x0	spy_align7[3:0]	SPY alignment control for SPY signal 7 (spy_out[7]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay
27:24	R/W	0x0	spy_align6[3:0]	SPY alignment control for SPY signal 6 (spy_out[6]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay

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SPY MICRO-ARCHITECTURE REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
23:20	R/W	0x0	spy_align5[3:0]	SPY alignment control for SPY signal 5 (spy_out[5]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay
19:16	R/W	0x0	spy_align4[3:0]	SPY alignment control for SPY signal 4 (spy_out[4]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay
15:12	R/W	0x0	spy_align3[3:0]	SPY alignment control for SPY signal 3 (spy_out[3]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay

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SPY MICRO-ARCHITECTURE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
11:8	R/W	0x0	spy_align2[3:0]	SPY alignment control for SPY signal 2 (spy_out[2]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay
7:4	R/W	0x0	spy_align1[3:0]	SPY alignment control for SPY signal 1 (spy_out[1]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay
3:0	R/W	0x0	spy_align0[3:0]	SPY alignment control for SPY signal 0 (spy_out[0]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay

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SPY MICRO-ARCHITECTURE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x04 100C			***DBG_SPY_ALIGN_REG1***	
31:16	R	NI	reserved	Read as 0.
15:12	R/W	0x0	spy_align11[3:0]	SPY alignment control for SPY signal 11 (spy_out[11]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay
11:8	R/W	0x0	spy_align10[3:0]	SPY alignment control for SPY signal 10 (spy_out[10]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay

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SPY MICRO-ARCHITECTURE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
7:4	R/W	0x0	spy_align9[3:0]	SPY alignment control for SPY signal 9 (spy_out[9]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay
3:0	R/W	0x0	spy_align8[3:0]	SPY alignment control for SPY signal 8 (spy_out[8]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay
Offset 0x04 1FF4			***Powerdown Register***	
31	R/W	0	POWER_DOWN	Powerdown indicator 1 = Powerdown 0 = Power up When this bit equals 1, no other registers are accessible.
30:0		-	Unused	
Offset 0x04 1FFC			***Module ID Register***	
31:16	R	0116	MOD_ID	Module ID Number
15:12	R	0	REV_MAJOR	Major revision
11:8	R	0	REV_MINOR	Minor revision
7:0	R	00	APP_SIZE	Aperture size is 0 = 4 kB.

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Boot Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.3)

BOOT REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x04 2000			***Boot Status***	
31:1	R	31'b0	Reserved	
0	R	0	Boot Status	1 = Boot over 0 = Boot in progress
Offset 0x04 2FFC			***Module ID***	
31:16	R	0x010A	Boot Module ID	These bits represent the Boot Module ID.
15:12	R	1	Major Revision	Major Revision number of the module
11:8	R	0	Minor Revision	Minor Revision number of the module
7:0	R	0	Aperture Size	Aperture Size is 4 kB.

Smartcard UART 1 Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.16)

SMARTCARD UART 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Note: bit [7], RIU bar, of register UCR1 must be set to 1 before any action on the Smartcard UART registers.				
Offset 0x04 3000			***Reset Register (RER)***	
31:16	W	0	Unused	
15	W	0	RS_DONE	Reset the bit DONE in Mixed Status Register. RS_DONE is automatically reset by hardware.
14	W	0	RS_BGT	Reset the bit BGT in Mixed Status Register. RS_BGT is automatically reset by hardware.
13	W	0	RS_OCH	Reset the bit OCH in Mixed Status Register. RS_OCH is automatically reset by hardware.
12	W	0	RS_DMAERR	Reset the bit DMA_ERR in Mixed Status Register. RS_DMAERR is automatically reset by hardware.
11	W	0	RS_DMAABORT	Reset the bit DMA_ABORT in Mixed Status Register. RS_DMAABORT is automatically reset by hardware.
10	W	0	RS_TO3	Reset the bit TO3 in UART Status Register. RS_TO3 is automatically reset by hardware.
9	W	0	RS_TO2	Reset the bit TO2 in UART Status Register. RS_TO2 is automatically reset by hardware.
8	W	0	RS_TO1	Reset the bit TO1 in UART Status Register. RS_TO1 is automatically reset by hardware.

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SMARTCARD UART 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
7	W	0	RS_EA	Reset the bit EA in UART Status Register. RS_EA is automatically reset by hardware.
6	W	0	RS_PE	Reset the bit PE in UART Status Register. RS_PR is automatically reset by hardware.
5	W	0	RS_OVR	Reset the bit OVR in UART Status Register. RS_OVR is automatically reset by hardware.
4	W	0	RS_FER	Reset the bit FE in UART Status Register. RS_FER is automatically reset by hardware.
3	W	0	RS_TBERBF	Reset the bit TBE/RBF in UART Status Register. RS_TBERBF is automatically reset by hardware.
2	W	0	RFI	Reset FIFO pointers. This bit is automatically reset by hardware.
1	W	0	RMS	Reset Mixed Status (RMS) register. When set, this bit clears bits OCH, DONE, DMA_ABORT, DMA_ERR and BGT in the MSR register. It is automatically reset by hardware. Note that bit BGT in MSR does not generate interrupts.
0	W	0	RUS	Reset UART Status (RUS) register. When set, this bit clears all bits in the USR register. This bit is automatically reset by hardware.
Offset 0x04 3004			***Clock Configuration Register (CCR)***	
7	R/W	0	SFD	When set to ‘1’, 1 ETU = 624 clock card cycles
6	R/W	0	RPB	Remove Parity Bit. When this bit is set to ‘1’: • In transmission mode: the parity bit is removed (allowing a 10 ETU data frame). • In reception mode: there is no parity error check.
5	R/W	0	SHL	When the bit CST (see below) is set to 1, then clock card signal (output CLOCK_CARD) is stopped low if SHL=0, and high if SHL=1.
4	R/W	0	CST	In case of an asynchronous card, the bit CST (Clock Stop) defines whether the clock card (output pin CLK_CARD) is stopped or not.
3	R/W	0	SC	In case of a synchronous card (bit SAN in UCR2 set to 1), the output CLK_CARD is a copy of the bit SC.

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SMARTCARD UART 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
2:0	R/W	0	AC2:AC0	If CST is reset (=0), then the clock card frequency (output CLK_CARD) is determined by those bits according to the following table: AC2: AC1: AC0 = 000: CLK_CARD = CORE_CLK/2 AC2: AC1: AC0 = 001: CLK_CARD = CORE_CLK/4 AC2: AC1: AC0 = 010: CLK_CARD = CORE_CLK/6 AC2: AC1: AC0 = 011: CLK_CARD = CORE_CLK/8 AC2: AC1: AC0 =1 00: CLK_CARD = CORE_CLK/12 AC2: AC1: AC0 =101: CLK_CARD = CORE_CLK/16 AC2: AC1: AC0 =110: CLK_CARD = CORE_CLK/24 AC2: AC1: AC0 =111: CLK_CARD = CORE_CLK/32 All frequency changes are synchronous, ensuring that no spike or unwanted pulse width occurs during changes.
Offset 0x04 3008			***Programmable Divider Register (PDR)***	
7:0	R/W	00000001	PD7:PD0	This register is used for counting the card clock cycles forming the ETUs. The value 00000000 should never be written in this register.
Offset 0x04 300C			***UART Configuration Register 2 (UCR2)***	
7	R/W	0	RSTIN	Card reset signal from the controller. The output pin RSTIN is a copy of this bit.
6	R/W	0	DISTBE/RBF	If bit DISTBE/RBF (disable TBE/RBF interrupt) is set, then reception or transmission of a character will not generate an interrupt.
5	R/W	0	START	If the controller sets START to 1, the card is activated. If the controller resets START to 0, the card is deactivated. The output CMDVCC = NOT (START). (see *TDA8004 data sheet Ref.9397 750 06034*)
4	R/W	0	DMAE	If bit DMAE (DMA enable) is set (=1), DMA mode is enable; when reset, interrupt mode is active.' The bit DMAE is automatically reset (= 0) by hardware in the following conditions: • DMA transfer successfully finished (bit DONE set in MSR) • A parity error occurred during the DMA mode in T= 0 protocol (bit PE set in USR) • A change occurred on input pad OFF (bit OCH set in MSR) • An error occurred on the PI-bus (bit DMA_ERR set in MSR).
3	R/W	0	SAN	Synchronous/Asynchronous is set by software if a synchronous card is expected. The UART is bypassed and only bits 0 in URR and in UTR are connected to I/O. In this case, CLK_CARD output is controlled by bit SC in the CCR register.
2	R/W	0	AUTOCONV	If bit $\overline{\text{AUTOCONV}}$ is set, the convention is set by software with bit CONV in the UCR1 register. If it is reset, the convention is automatically detected on the first received character while bit SS (Start Session) is set.
1	R/W	0	CKU	When bit CKU is set, one ETU will last to half of the formula below.

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SMARTCARD UART 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
0	R/W	0	PSC	If PSC is set high, the prescaler value is 32. If PSC is set low, the prescaler value is 31. One ETU will last the number of card clock cycles equal to PRESCALER x PDR.
Offset 0x04 3010			***DMA Read Address Register (DRA)***	
31:0	R/W	0	DRA[31:0]	It points at the memory at which the transfer is supposed to start when the UART is in transmission mode. This register must be programmed before setting the DMAE bit in UCR2.
Offset 0x04 3014			***Guard Time Register (GTR)***	
31:8		-	Unused	
7:0	R/W	0	GT[7:0]	This register is used to store the number of guard ETUs given by the card during ATR. In transmission mode, the UART will wait this number of ETUs before transmitting the character stored in UTR. In T=1 protocol, GTR=FF means operation at 11 ETUs. In protocol T=0, GTR=FF means operation at 12 ETUs. See *PNX8526 User Manual, Ref. UM10104_1, Chap.16)* for more details.
Offset 0x04 3018			***UART Configuration Register 1 (UCR1)***	
31:8		-	Unused	
7	R/W	0	RIU	Reset ISO UART ($\overline{\text{RIU}}$). This must be set to 1 before any action on the UART. When set to 0, this bit resets all UART registers to their initial value. UART is inactive if $\overline{\text{RIU}}$ = 0.
6	R/W	0	FIP	Force Inverse Parity 1 = The UART will NACK a correct received character and will transmit characters with wrong parity bits.
5	R/W	0	FC	Flow Control is set if the flow control is used.
4	R/W	0	PROT	Determines the protocol type when in asynchronous transmission. 0 = Protocol is T = 0 1 = Protocol is T = 1 In protocol T=1, if there is a parity error in reception mode the character is loaded and an interruption is generated but the DMA transfer is not aborted. In protocol T=0, when the parity error counter reaches its terminal count, the DMA transfer is aborted and the character is not loaded.
3	R/W	0	T/R	Transmit/Receive is set by software for transmission mode. A change from 0 to 1 will set the TBE bit in the USR. T/R is automatically reset by hardware if LCT has been used after transmitting the last character.
2	R/W	0	LCT	Last Character to Transmit is set by software after writing in the UART Transmit register (UTR) the last character to transmit. It allows automatic change to reception mode. Reset by hardware at the end of a successful transmission.
1	R/W	0	SS	Start Session is set before ATR for automatic convention detection and early answer detection (must be reset by software after reception of a correct initial character).

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SMARTCARD UART 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
0	R/W	0	CONV	Convention is set HIGH if the convention is direct, LOW in case of inverse convention. CONV is either automatically written by hardware according to the convention detected during ATR, or by software if the AUTOCONV bit is set.
Offset 0x04 301C			***DMA Length Register (DLR)***	
31:16	R/W	0	DLW[15:0]	Determines the number of characters (bytes) to be transferred in memory (65535 bytes max) when in reception mode. This register must be programmed before setting the DMAE bit in UCR2.
15:12		-	Unused	Read and write as zeroes.
11:0	R/W	0	DLR[11:0]	Determines the number of characters (bytes) to send (4095 bytes max) to the Smartcard when in transmission mode. This register must be programmed before setting the DMAE bit in UCR2.
Offset 0x04 3020			***Time Out Configuration Register (TOC)***	
31:8		-	Unused	
7:6	R/W	0	MODE31, MODE30	Counter3 mode control 00 = STOP: the counter stops counting. 01 = AUTORELOAD: the counter starts counting the value stored in the associated register on the first start bit after this mode has been programmed, and automatically restarts counting this value when it has reached the terminal count. An interrupt is generated at every terminal count. 10 = SOFTWARE TRIGGERED: the counter starts counting the value stored in the associated registers. When the counter reaches its terminal count, it generates an interrupt and stops. The mode bits are reset to (0,0) by hardware. 11 = TRIGGERED ON START BIT ON I/O: In this mode, the counter will automatically start counting the value stored in the associated registers when a start bit occurs on I/0 (reception or transmission). An interrupt is only generated if the counter reaches the terminal count. Then the counter is stopped. The mode bits are reset to (0,0) by hardware.
5:4	R/W	0	MODE21, MODE20	Counter2 mode control Same as the Counter3 mode control [7:6] described above.
3:2	R/W	0	MODE11, MODE10	Counter1 mode control Same as the Counter3 mode control [7:6] described above.
1:0	R/W	0	8/16, 16/24	00 = TOR3, TOR2 and TOR1 are linked as a 24-bit ETU counter 01 = TOR3 and TOR2 are linked as a 16-bit ETU counter and TOR1 is an independent 8-bit ETU counter. 1X = TOR3, TOR2 and TOR1 are 3 independent 8-bit ETU counters
Offset 0x04 3024			***Time Out Register 1 (TOR1)***	
31:8		-	Unused	

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SMARTCARD UART 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
7:0	W	0	TOL[7:0]	8-bit ETU counter. Can be linked to TOR2 and TOR3 registers to form a 24-bit ETU counter (see the TOC register description for more information)
Offset 0x04 3028			***Time Out Register 2 (TOR2)***	
31:8		-	Unused	
7:0	W	0	TOL[15:8]	8-bit ETU counter. Can be linked: • to TOR1 and TOR3 registers to form a 24-bit ETU counter • to TOR3 only to form a 16-bit ETU counter (see the TOC register description for more information)
Offset 0x04 302C			***Time Out Register 3 (TOR3)***	
31:8		-	Unused	
7:0	W	0	TOL[23:16]	8-bit ETU counter. Can be linked: • to TOR1 and TOR2 registers to form a 24-bit ETU counter • to TOR2 only to form a 16-bit ETU counter (see the TOC register description for more information.)
Offset 0x04 3030			***Mixed Status Register (MSR)***	
31:8		-	Unused	
7	R	0	DONE	1 = DMA transfer ended successfully. When this bit is set, INT goes high. The bit is reset when the RMS bit is set in Reset register.
6	R	0	FE	FIFO Empty 1 = The reception FIFO is empty. The bit is reset when at least one character has been loaded in the FIFO.
5	R	0	BGT	The BGT bit is linked with a 22-ETU counter, which is started at every start bit on I/O. If the count is finished before the next start bit, the BGT bit is set. This helps check that the card has not answered before 22 ETUs after the last transmitted character, or transmitted a character before 22 ETUs after the last received character. This bit is reset by setting the RMS bit in the Reset register.
4	R	0	BOF	The $\overline{\text{BOF}}$ bit is a copy of the pin $\overline{\text{OFF}}$.
3	R	0	OCH	1 = A change occurred on pin $\overline{\text{OFF}}$. When this bit is set, INT goes high. The bit is reset when the RMS bit is set in the Reset register.
2	R	0	DMA_ERR	1 = A problem occurred on the PI bus during a transaction (timeout, wrong memory address...). In that case the DMA transfer is aborted and the DMA_ABORT status bit is also set.
1	R	0	DMA_ABORT	1 = An anomaly occurred during a DMA transfer (Parity Error counter reaches its terminal count, OCH and DMA_ERROR). When DMA_ABORT is set, then the DMAE bit in UCR2 is reset (DMA transfer stopped).

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SMARTCARD UART 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
0	R	0	TBE/RBF	Transmit buffer empty/receive buffer full. 1 = One of the following occurred: • Change from reception mode to transmission mode • A character has been transmitted by the UART • The reception FIFO is full The TBE/RBF bit is reset when the $\overline{\text{RIU}}$ bit is reset, or when a character has been written in UTR, or when the RUR bit in the Command Register (CRE) is set HIGH, or when changing from transmission mode to reception mode.
Offset 0x04 3030			***FIFO Control Register (FCR)***	
31:7		-	Unused	
6:4	W	0	PEC[2:0]	PEC2, PEC1 and PEC0 determine the number of accepted parity errors before setting the PE (Parity Error) bit within the UART Status Register (USR) and setting INT high in protocol T=0 000 = Only 1 parity error will be accepted 111 = 8 parity errors will be accepted
3		-	Unused	
2:0	W	0	FL[2:0]	FL[2:0] determines the depth of the FIFO 000 = Length 1 111 = Length 8 When DMA is enabled FL[2:0] must be 000.
In protocol T=0, if a correct character is received before the programmed error number is reached, then the error counter is reset. If the programmed number of allowed parity errors is reached, then the PE bit within the UART Status Register (USR) is set as long as the RUS bit in the Reset register has not been set. In protocol T=1, the error counter has no action. (PE is set at the first wrong received character). When DMA is enabled (DMAE bit set in UCR2), bits FL[2:0] must be reset.				
Offset 0x04 3034			***UART Transmit Register (UTR)***	
31:8		-	Unused	
7:0	W	0	UT[7:0]	To transmit a character to the card, the controller writes the data to this register in direct convention. The transmission: • starts at the end of this writing if the previous character has been transmitted and the extra guard time has expired • starts at the end of the extra guard time (if it has not expired) • does not start if the transmission of the previous character is not completed In synchronous mode, the UT0 data is written on the I/O line of the card when the UTR has been written and remains unchanged.
Offset 0x04 3034			***UART Receive Register (URR)***	
31:8		-	Unused	

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SMARTCARD UART 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
7:0	R	0	UR[7:0]	To read data from the card, the controller reads it from this register in direct convention. When needed, this register may be tied to the FIFO whose length n is programmable between 1 and 8 (see bit FL[2:0] in FIFO Control register). Reading this register does not affect the UART, which means the TBE/RBF bits present in the USR & MSR registers are not affected and FIFO pointers are not updated. To update the UART, the controller must set the RUR bit in the Command register. In synchronous mode, the UR0 bit is directly linked to the I/O line of the card.
Offset 0x04 3038			***UART Status Register (USR)***	
This register is used by the controller to monitor the activity of the ISO UART and timeout counters.				
31:8		-	Unused	
7:5	R	0	TO[3:1]	Bit TO1 is set when counter1 has reached its terminal count. Bit TO2 is set when counter2 has reached its terminal count. Bit TO3 is set when counter3 has reached its terminal count.
4	R	0	EA	Early Answer is high if the first start bit on I/O DURING ATR has been detected between 200 and 384 CLK card pulses (all activities on I/O line during the first 200 CLK card pulses with RST low or high are not taken into account).
3	R	0	PE	Parity Error (see bits PEC2:PEC0 in FIFO Control register).
2	R	0	OVR	Overrun is high if the UART has received a new character while the URR was full. In this case, at least one character has been lost.
1	R	0	FER	Framing Error is high when I/O was not in high impedance state at 10.25 ETUs after a start bit.
0	R	0	TBE/RBF	Transmission Buffer Empty is 1 when the UART is in transmission mode and when the controller may write the next character to transmit in UTR. It is reset when the controller has written data in the transmit register or when the T/R bit within UCR1 has been reset either automatically or by software. Reception Buffer Full is high when the FIFO is full. The controller may set the RUR bit in the Command register which clears the RBF bit after it has read the URR register. TBE and RBF share the same bit within the USR. (When in transmission mode, TBE is relevant; when in reception mode, RBF is relevant.)

In T=0 protocol, PE is high if the UART has detected a number of received characters with parity error equal to the number written in PEC2, PEC1 and PEC0, or if a transmitted character has been NACKed by the card.

In T=0 protocol, a character received with a parity error is not stored in the FIFO. In T=1 protocol, a character with parity error is stored in the FIFO and the parity error counter is not operating.

If any of the status bits FER, OVR, PE, EA, TO1, TO2 and TO3 is set, then INT is high. The bit having caused the interrupt is reset when the RUS bit is set in the Reset register. If TBE/RBF is set, and if the mask bit DISTBE/RBF within the UCR2 is not set, then INT is also high. TBE/RBF is reset when data has been written in the UTR, or when the RUR bit is set in the Command register, or when changing from transmission mode to reception mode.

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SMARTCARD UART 1 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x04 303C			*DMA Write Address Register (DWA)*	
31:0	R/W	0	DWA[31:0]	Points to the memory address at which the transfer is supposed to start (32-bit register) when the UART is in reception mode. This register must be programmed before setting the DMAE bit in UCR2. DMA buffers have to start on a word-aligned boundary.
Offset 0x04 3040			*Command Register (CRE)*	
31:4		-	Unused	
3	W	0	RAF	Reset the DMA gate autoflush mode.
2	W	0	SDA	When this bit is set to 1, DMA gate autoflush mode is enable. (DMA gate autoflush mode: When in reception mode, the DMA gate is automatically flushed if no character have been received 100 us after the last received character).
1	W	0	FDG	Flushes the UART DMA Gate. It is automatically reset by hardware.
0	W	0	RUR	After reading the UART Receive register, the controller may set this bit in order to update: • the FIFO pointers • TBE/RBF bits in USR and MSR registers (in reception mode)
Offset 0x04 3FE0			*SCIF_INT_STATUS*	
31:12		-	Unused	
11	R	0	DONE	See description in Mixed Status Register (MSR).
10	R	0	OCH	See description in Mixed Status Register (MSR).
9	R	0	DMA_ERR	See description in Mixed Status Register (MSR).
8	R	0	DMA_ABORT	See description in Mixed Status Register (MSR).
7	R	0	TO3	See description in UART Status Register (USR).
6	R	0	TO2	See description in UART Status Register (USR).
5	R	0	TO1	See description in UART Status Register (USR).
4	R	0	EA	See description in UART Status Register (USR).
3	R	0	PE	See description in UART Status Register (USR).
2	R	0	OVR	See description in UART Status Register (USR).
1	R	0	FER	See description in UART Status Register (USR).
0	R	0	TBE/RBF	See description in UART Status Register (USR).
Offset 0x04 3FE4			*SCIF_INT_ENABLE*	
31:12		-	Unused	
11	R/W	0	ENA_DONE	Enable DONE interrupt.
10	R/W	0	ENA_OCH	Enable OCH interrupt.
9	R/W	0	ENA_DMA_ERR	Enable DMA_ERR interrupt.
8	R/W	0	ENA_DMA_ABORT	Enable DMA_ABORT interrupt.
7	R/W	0	ENA_TO3	Enable TO3 interrupt.

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SMARTCARD UART 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
6	R/W	0	ENA_TO2	Enable TO2 interrupt.
5	R/W	0	ENA_TO1	Enable TO1 interrupt.
4	R/w	0	ENA_EA	Enable EA interrupt.
3	R/W	0	ENA_PE	Enable PE interrupt.
2	R/W	0	ENA_OVR	Enable OVR interrupt.
1	R/W	0	ENA_FER	Enable FER interrupt.
0	R/W	0	ENA_TBE/RBF	Enable TBE/RBF interrupt.
Offset 0x04 3FE8			***SCIF_INT_CLEAR***	
31:12		-	Unused	
11	W	0	CLR_DONE	Write 1 to clear DONE interrupt.
10	W	0	CLR_OCH	Write 1 to clear OCH interrupt.
9	W	0	CLR_DMA_ERR	Write 1 to clear DMA_ERR interrupt.
8	W	0	CLR_DMA_ABORT	Write 1 to clear DMA_ABORT interrupt.
7	W	0	CLR_TO3	Write 1 to clear TO3 interrupt.
6	W	0	CLR_TO2	Write 1 to clear TO2 interrupt.
5	W	0	CLR_TO1	Write 1 to clear TO1 interrupt.
4	W	0	CLR_EA	Write 1 to clear EA interrupt.
3	W	0	CLR_PE	Write 1 to clear PE interrupt.
2	W	0	CLR_OVR	Write 1 to clear OVR interrupt.
1	W	0	CLR_FER	Write 1 to clear FER interrupt.
0	W	0	CLR_TBE/RBF	Write 1 to clear TBE/RBF interrupt.
Offset 0x04 3FEC			***SCIF_INT_SET***	
31:12		-	Unused	
11	W	0	SET_DONE	Set DONE interrupt.
10	W	0	SET_OCH	Set OCH interrupt.
9	W	0	SET_DMA_ERR	Set DMA_ERR interrupt.
8	W	0	SET_DMA_ABORT	Set DMA_ABORT interrupt.
7	W	0	SET_TO3	Set TO3 interrupt.
6	W	0	SET_TO2	Set TO2 interrupt.
5	W	0	SET_TO1	Set TO1 interrupt.
4	W	0	SET_EA	Set EA interrupt.
3	W	0	SET_PE	Set PE interrupt.
2	W	0	SET_OVR	Set OVR interrupt.
1	W	0	SET_FER	Set FER interrupt.
0	W	0	SET_TBE/RBF	Set TBE/RBF interrupt.
Offset 0x04 3FF4			***SCIF_POWERDOWN***	

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SMARTCARD UART 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
31	R/W	0	PWDN	When set, access to Smartcard Interface registers is forbidden, except for SCIF_MODULE_ID and SCIF_POWERDOWN.
30:0		-	Unused	
Offset 0x04 3FFC			***SCIF_MODULE_ID***	
31:16	R	0x0106	MODULE_ID	Smartcard Interface ID code
15:12	R	1	REV_MAJOR	Major revision
11:8	R	0	REV_MINOR	Minor revision
7:0	R	0	APP_SIZE	Aperture size is 0 = 4 kB.

Smartcard UART 2 Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.16)

SMARTCARD UART 2 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Smartcard Registers 1 (Offset 0x04 3000) and Smartcard Registers 2 (Offset 0x04 4000) The Smartcard registers 1 and 2 are identical except for their offsets. A duplicate set has been created to facilitate programming. The table for Smartcard registers 1(0x04 3000) precedes this table.				
Offset 0x04 4000			***Reset Register (RER)***	
Offset 0x04 4004			***Clock Configuration Register (CCR)***	
Offset 0x04 4008			***Programmable Divider Register (PDR)***	
Offset 0x04 400C			***UART Configuration Register 2 (UCR2)***	
Offset 0x04 3010			***DMA Read Address Register (DRA)***	
Offset 0x04 4014			***Guard Time Register (GTR)***	
Offset 0x04 4018			***UART Configuration Register 1 (UCR1)***	
Offset 0x04 401C			***DMA Length Register (DLR)***	
Offset 0x04 4020			***Timeout Configuration Register (TOC)***	
Offset 0x04 4024			***Timeout Register 1 (TOR1)***	
Offset 0x04 4028			***Timeout Register 2 (TOR2)***	
Offset 0x04 402C			***Timeout Register 3 (TOR3)***	
Offset 0x04 4030			***Mixed Status Register (MSR)***	
Offset 0x04 4030			***FIFO Control Register (FCR)***	
Offset 0x04 4034			***UART Transmit Register (UTR)***	
Offset 0x04 4034			***UART Receive Register (URR)***	
Offset 0x04 4038			***UART Status Register (USR)***	
Offset 0x04 403C			***DMA Write Address Register (DWA)***	
Offset 0x04 4040			***Command Register (CRE)***	
Offset 0x04 4FE0			***SCIF_INT_STATUS***	

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SMARTCARD UART 2 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x04 4FE4			*SCIF_INT_ENABLE*	
Offset 0x04 4FE8			*SCIF_INT_CLEAR*	
Offset 0x04 4FEC			*SCIF_INT_SET*	
Offset 0x04 4FF4			*SCIF_POWERDOWN*	
Offset 0x04 4FFC			*SCIF_MODULE_ID*	

I²C Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.15)

I²C 1 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
I2C 1 Registers (Offset 0x04 5000) and I2C 2 Registers (Offset 0x04 6000) The I2C 1 and 2 registers are identical except for their offsets. A duplicate set has been created to facilitate programming. The table for I2C 2 registers (0x04 6000) follows this table.				
See Ch 17 for more details on these registers.				
Offset 0x04 5000			*I2C CONTROL*	
31:8		-	Unused	Ignore upon read. Write as zeroes.
7	R/W	0	AA	I2C acknowledge bit 0 = Acknowledge not returned during acknowledge clock pulse. 1 = Acknowledge returned during acknowledge clock pulse.
6	R/W	0	EN	I2C enable bit 0 = Disable I2C module. 1 = Enable I2C module.
5	R/W	0	STA	I2C start bit 0 = Slave mode, accept transactions. 1 = Master mode, generate start condition if bus is free.
4	R	0	STO	I2C stop bit 0 = Slave mode, accept transactions. 1 = Generate stop condition on I2C bus when I2C module is master.
3		-	Unused	Ignore upon read. Write as zeroes.

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I²C 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
2:0	R/W	000	CR2	These three bits determine the serial clock frequency. The 12 MHz I2C Clock is divided to achieve the desired frequency. [2:0]DividerFrequency (kHz) 00060400 00180300 010120200 011160150 100240100 10132075 11048050 11196025
Offset 0x04 5004			***I2C DATA REGISTER***	
31:8		-	Unused	Ignore upon read. Write as zeroes.
7:0	R/W	0	DAT	Write byte data to be transmitted on the I2C bus. Read byte data has been received from the I2C bus.
Offset 0x04 5008			***I2C STATUS REGISTER***	
31:8		-	Unused	Ignore upon read. Write as zeroes.
7:3	R	11111	STA	Indicates the status of the I2C module.
2:0		-	Unused	Ignore upon read. Write as zeroes.
Offset 0x04 500C			***I2C ADDRESS REGISTER***	
31:8		-	Unused	Ignore upon read. Write as zeroes.
7:1	R/W	0x00	SLAVE_ADDR	Slave address when in slave mode
0	R/W	0x0	GEN_CALL_ADDR	General call address 0 = Does not generate interrupt if general call address is detected on the I2C bus. 1= Generates interrupt if general call address is detected.
Offset 0x04 5010			***I2C STOP REGISTER***	
31:1		-	Unused	Ignore upon read. Write as zeroes.

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I²C 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
0	R/W	0	STO	Set and read STO flag Writes: In master mode, set STO flag to indicate a STOP has been requested. Then generate a STOP condition on I2C bus. When the STOP condition is detected on the bus, the I2C module hardware clears the STO flag. In slave mode, set STO flag to indicate a STOP has been requested. No STOP condition is transmitted to the I2C bus. However, the I2C module hardware behaves as if a STOP condition has been received and switches to the defined “not addressed” slave receiver mode. The STO flag is immediately cleared by the hardware so that software can never see it set. Reads: View the STO flag to see if a STOP has been requested. STO flag can also be viewed by reading the STO bit of IIC_CONTROL. See STO bit of IIC_CONTROL register for more information
Offset 0x04 5014			***I2C PD REGISTER***	
31:3		-	Unused	Ignore upon read. Write as zeroes.
2	R/W	0	PD	This bit synchronously resets the I2C clock domain except for the MMIO registers. 0 = Don’t reset I2C clock domain. 1 = Reset I2C clock domain. Note: Do not reset the I2C clock domain until the I2C module is disabled using bit 6 of the I2C Control register.
1:0		-	Unused	Ignore upon read. Write as zeroes.
Offset 0x04 5018			***I2C BUS SET REGISTER***	
31:2		-	Unused	Ignore upon read. Write as zeroes.
1	W	0	SET_SCL_LOW	Pull I2C SCL bus signal to logic one or zero: 1 = Pulls SCL signal to logic zero. 0 = SCL signal is not pulled to logic zero.
0	W	0	SET_SDA_LOW	Pull I2C SDA bus signal to logic one or zero: 1 = Pulls SDA signal to logic zero. 0 = SDA signal is not pulled to logic zero.
Offset 0x04 501C			***I2C BUS OBSERVATION REGISTER***	
31:2		-	Unused	Ignore upon read. Write as zeroes.
1	R	0	OBSERVE_SCL	Observe I2C SCL bus signal: 1 = SCL signal is at logic one. 0 = SCL signal is at logic zero.
0	R	0	OBSERVE_SDA	Observe I2C SDA bus signal 1 = SDA signal is at logic one. 0 = SDA signal is at logic zero.
Offset 0x04 5020—5FDC			***Reserved***	

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I²C 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x04 5FE0			***I2C INTERRUPT STATUS REGISTER***	
31:1		-	Unused	Ignore upon read. Write as zeroes.
0	R	0	INT_STATUS	Interrupt status register. It reports any pending interrupts: 1 = Interrupt i pending. 0 = Interrupt i not pending.
Offset 0x04 5FE4			***I2C INTERRUPT ENABLE REGISTER***	
31:1		-	Unused	Ignore upon read. Write as zeroes.
0	R/W	0	INT_ENABLE	Interrupt enable register 1 = Interrupt i is enabled. 0 = Interrupt is disabled.
Offset 0x04 5FE8			***I2C INTERRUPT CLEAR REGISTER***	
31:1		-	Unused	Ignore upon read. Write as zeroes.
0	W	0	INT_CLEAR	Interrupt clear register. 1 = Interrupt is cleared. 0 = Interrupt is not cleared.
Note: The I²C module will look at a new transaction on the I²C bus as soon as the previous interrupt has been cleared. Therefore, software must make sure that “interrupt clear” is the last transaction that is sent to the I²C module before starting a new transaction.				
Offset 0x04 5FEC			***I2C INTERRUPT SET REGISTER***	
31:1		-	Unused	Ignore upon read. Write as zeroes.
0	W	0	INT_SET	Interrupt set register. Allows software to set interrupts. 1 = Interrupt is set. 0 = Interrupt is not set.
Offset 0x04 5FF4			***I2C POWERDOWN REGISTER***	
31	R/W	0	POWER_DOWN	0 = Normal operation of peripheral. This is the reset value. 1 = Module is powerdown and module clock can be removed. Module returns DEADABBA on all reads except for reads of the powerdown bit. Module generates ERR ACK on all writes except for writes to the powerdown bit.
30:0		-	Unused	Ignore upon read. Write as zeroes.
Offset 0x04 5FFC			***I2C MODULE ID REGISTER***	
31:16	R	0x0105	MODULE ID	Unique 16-bit code. Module ID 0 and -1 are reserved for future use.
15:12	R	0	MAJREV	Major Revision
11:8	R	1	MINREV	Minor Revision
7:0	R	0	MODULE APERTURE SIZE	Aperture size = 4 kB*(bit_value+1), so 0 means 4 kB (the default).

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I^2C 2 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
I2C 1 Registers (Offset 0x04 5000) AND I2C 2 Registers (Offset 0x04 6000) The I2C 1 and 2 registers are identical except for their offsets. A duplicate set has been created to facilitate programming. The table for I2C 1 registers (0x04 5000) precedes this table.				
Offset 0x04 6000			*I2C CONTROL*	
Offset 0x04 6004			*I2C DATA REGISTER*	
Offset 0x04 6008			*I2C STATUS REGISTER*	
Offset 0x04 600C			*I2C ADDRESS REGISTER*	
Offset 0x04 6010			*I2C STOP REGISTER*	
Offset 0x04 6014			*I2C PD REGISTER*	
Offset 0x04 6018			*I2C BUS SET REGISTER*	
Offset 0x04 601C			*I2C BUS OBSERVATION REGISTER*	
Offset 0x04 6020—5FDC			*Reserved*	
Offset 0x04 6FE0			*I2C INTERRUPT STATUS REGISTER*	
Offset 0x04 6FE4			*I2C INTERRUPT ENABLE REGISTER*	
Offset 0x04 6FE8			*I2C INTERRUPT CLEAR REGISTER*	
Offset 0x04 6FEC			*I2C INTERRUPT SET REGISTER*	
Offset 0x04 6FF4			*I2C POWERDOWN REGISTER*	
Offset 0x04 6FFC			*I2C MODULE ID REGISTER*	

Clock Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.5)

CLOCK REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Clock Control				
Offset 0x04 7000			*PLL0_CTL*	
Reset values are set for expected frequencies for faster boot-up, shorter boot code. Note: When this register is written, PI_ACK must be held in “WAT” until blocking of the clock has started.				
31	R	n/a	pll0_blocked	1 = blocking of clock from the PLL is in progress
30:26	R/W	n/a	Reserved	Read as 0, write nothing
25	R/W	0	sel_pwrdwn_clk_mem	1 = select XTAL_CLK/16 as source clock for clk_mem - this is used in powerdown mode to slow down clk_mem. NOTE: to slow down clk_fpi, clk_mips, clk_mpi & clk_tpi, CLK_FPI_CTL must be set to hex00000005
24:16	R/W	23h	pll0_n	9-bit N parameter to PLL0
15:13	R/W	n/a	Reserved	Read as 0, write nothing
12:8	R/W	3h	pll0_m	5-bit M parameter to PLL0

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CLOCK REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
7:4	R/W	n/a	Reserved	Read as 0, write nothing
3:2	R/W	1h	pll0_p	2-bit P parameter to PLL0. The programming values for P are: 00: P=1, 01: P=2, 10: P=2, 11: P=4
1	R/W	0	pll0_pd	1 = powerdown PLL0
0	R/W	n/a	Reserved	Read as 0, write nothing
Offset 0x04 7004			***PLL1_CTL***	
Reset values are set for expected frequencies for faster boot-up, shorter boot code. Note: When this register is written, PI_ACK must be held in “WAT” until blocking of the clock has started				
31	R	n/a	pll1_blocked	1 = blocking of clock from the PLL is in progress
30:25	R/W	n/a	Reserved	Read as 0, write nothing
24:16	R/W	23h	pll1_n	9-bit N parameter to PLL1
15:13	R/W	n/a	Reserved	Read as 0, write nothing
12:8	R/W	3h	pll1_m	5-bit M parameter to PLL1
7:4	R/W	n/a	Reserved	Read as 0, write nothing
3:2	R/W	1h	pll1_p	2-bit P parameter to PLL1. The programming values for P are: 00: P=1, 01: P=2, 10: P=2, 11: P=4
1	R/W	0	pll1_pd	1 = powerdown PLL1
0	R/W	n/a	Reserved	Read as 0, write nothing
Offset 0x04 7008			***PLL2_CTL***	
Reset values are set for expected frequencies for faster boot-up, shorter boot code. Note: When this register is written, PI_ACK must be held in “WAT” until blocking of the clock has started				
31	R	n/a	pll2_blocked	1 = blocking of clock from the PLL is in progress
30:25	R/W	n/a	Reserved	Read as 0, write nothing
24:16	R/W	23h	pll2_n	9-bit N parameter to PLL2
15:13	R/W	n/a	Reserved	Read as 0, write nothing
12:8	R/W	3h	pll2_m	5-bit M parameter to PLL2
7:4	R/W	n/a	Reserved	Read as 0, write nothing
3:2	R/W	1h	pll2_p	2-bit P parameter to PLL2. The programming values for P are: 00: P=1, 01: P=2, 10: P=2, 11: P=4
1	R/W	0	pll2_pd	1 = powerdown PLL2
0	R/W	n/a	Reserved	Read as 0, write nothing
Offset 0x04 700C			***PLL3_CTL***	
Reset values are set for expected frequencies for faster boot-up, shorter boot code. Note: When this register is written, PI_ACK must be held in “WAT” until blocking of the clock has started				
31	R	n/a	pll3_blocked	1 = blocking of clock from the PLL is in progress
30:25	R/W	n/a	Reserved	Read as 0, write nothing
24:16	R/W	23h	pll3_n	9-bit N parameter to PLL3

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CLOCK REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
15:13	R/W	n/a	Reserved	Read as 0, write nothing
12:8	R/W	3h	pll3_m	5-bit M parameter to PLL3
7:4	R/W	n/a	Reserved	Read as 0, write nothing
3:2	R/W	1h	pll3_p	2-bit P parameter to PLL3. The programming values for P are: 00: P=1, 01: P=2, 10: P=2, 11: P=4.
1	R/W	0	pll3_pd	1 = powerdown PLL3
0	R/W	n/a	Reserved	Read as 0, write nothing
Offset 0x04 7010			***PLL4_CTL***	
31	R	n/a	pll4_blocked	1 = blocking of clock from the PLL is in progress
30:25	R/W	n/a	Reserved	Read as 0, write nothing
24:16	R/W	1Eh	pll4_n	9-bit N parameter to PLL4
15:13	R/W	n/a	Reserved	Read as 0, write nothing
12:8	R/W	2h	pll4_m	5-bit M parameter to PLL4
7:4	R/W	n/a	Reserved	Read as 0, write nothing
3:2	R/W	3h	pll4_p	2-bit P parameter to PLL4. The programming values for P are: 00: P=1, 01: P=2, 10: P=2, 11: P=4
1	R/W	0	pll4_pd	1 = powerdown PLL4
0	R/W	0	pll4_bp	1 = bypass PLL4
Offset 0x04 7014			***PLL5_CTL***	
31	R	n/a	pll5_blocked	1 = blocking of clock from the PLL is in progress
30:25	R/W	n/a	Reserved	Read as 0, write nothing
24:16	R/W	1Eh	pll5_n	9-bit N parameter to PLL5
15:13	R/W	n/a	Reserved	Read as 0, write nothing
12:8	R/W	2h	pll5_m	5-bit M parameter to PLL5
7:4	R/W	n/a	Reserved	Read as 0, write nothing
3:2	R/W	3h	pll5_p	2-bit P parameter to PLL5. The programming values for P are: 00: P=1, 01: P=2, 10: P=2, 11: P=4
1	R/W	0	pll5_pd	1 = powerdown PLL5
0	R/W	0	pll5_bp	1 = bypass PLL5
Offset 0x04 7018			***PLL1_7GHZ_CTL***	
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2	R/W	0	pll1_7ghz_pd	1 = powerdown PLL1_7GHZ
1:0	R/W	n/a	Reserved	Read as 0, write nothing
Offset 0x04 701C—709C			***RESERVED***	
Offset 0x04 7100			***DDS0_ICP1_CTL***	
31:0	R/W	0400-0000h	dds0_icp1_ctl[31:0]	32-bit DDS0 control (default = 27MHz)

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CLOCK REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x04 7104			***DDS1_ICP2_CTL***	
31:0	R/W	0400-0000h	dds1_icp2_ctl[31:0]	32-bit DDS1 control (default = 27MHz)
Offset 0x04 7108			***DDS2_AI1_CTL***	
31:0	R/W	05ED-097Bh	dds2_ai1_ctl[31:0]	32-bit DDS2 control (default = 40MHz)
Offset 0x04 710C			***DD3_AO1_CTL***	
31:0	R/W	05ED-097Bh	dds3_ao1_ctl[31:0]	32-bit DDS3 control (default = 40MHz)
Offset 0x04 7110			***DDS4_AI2_CTL***	
31:0	R/W	05ED-097Bh	dds4_ai2_ctl[31:0]	32-bit DDS4 control (default = 40MHz)
Offset 0x04 7114			***DDS5_AO2_CTL***	
31:0	R/W	05ED-097Bh	dds5_ao2_ctl[31:0]	32-bit DDS5 control (default = 40MHz)
Offset 0x04 7118			***DDS6_AIO3_CTL***	
31:0	R/W	05ED-097Bh	dds6_aio3_ctl[31:0]	32-bit DDS6 control (default = 40MHz)
Offset 0x04 711C			***DDS7_SPDO_CTL***	
31:0	R/W	00E9-0452h	dds7_spdo_ctl[31:0]	32-bit DDS7 control (default = 128*48kHz = 6.14MHz)
Offset 0x04 7120			***DDS8_TSDMA_CTL***	
31:0	R/W	038E-38E3h	dds8_tsdma_ctl[31:0]	32-bit DDS8 control (default = 24MHz)
Offset 0x04 7124—719C			***RESERVED***	
Offset 0x04 7200			***CLK_MEM_CTL***	
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:1	R/W	0h	sel_clk_mem	10 = sel_ext_clk_mem - clk_mem = GPIO[3] 01 = exit_rst_clk_mem - clk_mem = functional clock (PLL0) 00 = clk_mem = 27MHz xtal_clk
0	R/W	1	en_clk_mem	1 = enable clk_mem
Offset 0x04 7204			***CLK_FPI_CTL***	
31:4	R/W	n/a	Reserved	Read as 0, write nothing
3:1	R/W	0h	sel_clk_fpi	100 = sel_ext_clk_fpi - clk_fpi = GPIO[4] 010 = sel_clk_mem_fpi - source of clk_fpi is clk_mem 001 = exit_rst_clk_fpi - source of clk_fpi is PLL1 000 = clk_fpi = 27MHz xtal_clk
0	R/W	1	en_clk_fpi	1 = enable clk_fpi
Offset 0x04 7208			***Reserved***	
Offset 0x04 720C			***CLK_TPI_CTL***	

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CLOCK REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
31:2	R/W	n/a	Reserved	Read as 0, write nothing
1	R/W	0	exit_rst_clk_tpi	0 = clk_tpi = 27MHz xtal_clk 1 = clk_tpi = functional clock
0	R/W	1	en_clk_tpi	1 = enable clk_tpi
Offset 0x04 7210			***CLK_MPI_CTL***	
31:2	R/W	n/a	Reserved	Read as 0, write nothing
1	R/W	0	exit_rst_clk_mpi	0 = clk_mpi = 27MHz xtal_clk 1 = clk_mpi = functional clock
0	R/W	1	en_clk_mpi	1 = enable clk_mpi
Offset 0x04 7214			***Reserved***	
Offset 0x04 7218			***CLK_VMPG_CTL***	
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:1	R/W	0h	sel_clk_vmpg	10 = sel_ext_clk_vmpg - clk_vmpg = GPIO[6] 01 = exit_rst_clk_vmpg - clk_vmpg = functional clock 00 = clk_vmpg = 27MHz xtal_clk
0	R/W	1	en_clk_vmpg	1 = enable clk_vmpg
Offset 0x04 721C			***CLK_D2D_CTL***	
31:8	R/W	n/a	Reserved	Read as 0, write nothing
7	R/W	1	div_clk_d2d_pd	1 = powerdown clk_d2d divider in the CAB
6:5	R/W	n/a	Reserved	Read as 0, write nothing
4	R/W	1	div_clk_d2d	Divide clk_d2d: 0 = 86.4MHz - divide 1.728GHz by 20 1 = 108MHz - divide 1.728GHz by 16
3:1	R/W	0h	sel_clk_d2d	100 = sel_ext_clk_d2d - clk_d2d = UA1_TX 010 = sel_clk_mbs_d2d - select clk_mbs input 001 = exit_rst_clk_d2d - clk_d2d = functional clock 000 = clk_d2d = 27MHz xtal_clk
0	R/W	1	en_clk_d2d	1 = enable clk_d2d
Offset 0x04 7220			***CLK_VIP1_CTL***	
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2	R/W	0h	sel_invert_clk_vip1	1 = select inverted functional clock
1	R/W	0h	exit_rst_clk_vip1	0 = clk_vip1 = 27MHz xtal_clk 1 = clk_vip1 = functional clock
0	R/W	1	en_clk_vip1	1 = enable clk_vip1
Offset 0x04 7224			***CLK_VIP2_CTL***	
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2	R/W	0h	sel_invert_clk_vip2	1 = select inverted functional clock

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CLOCK REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
1	R/W	0h	exit_rst_clk_vip2	0 = clk_vip2 = 27MHz xtal_clk 1 = clk_vip2 = functional clock
0	R/W	1	en_clk_vip2	1 = enable clk_vip2
Offset 0x04 7228			***CLK_SMART1_CTL***	
(N.B: CLK_TSTAMP_CTL.div_clk_tstamp_pd must be set to '0' for clk_smart1 functional clock to work)				
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:1	R/W	0h	sel_clk_smart1	10 = sel_ext_clk_clk_smart: clk_smart = ext cclock 01 = exit_rst_clk_smart1: clk_smart = functional clock 00 = clk_smart = 27MHz xtal_clk
0	R/W	1	en_clk_smart	1 = enable clk_smart
Offset 0x04 722C			***CLK48_CTL***	
31:4	R/W	n/a	Reserved	Read as 0, write nothing
3	R/W	1	div_clk48_pd	1 = powerdown clk48 divider in the CAB
2:1	R/W	0h	sel_clk48	10 = sel_ext_clk48 - clk48 = GPIO[8] 01 = exit_rst_clk48 - clk48 = functional clock 00 = clk48 = 27MHz xtal_clk
0	R/W	1	en_clk48	1 = enable clk48
Offset 0x04 7230			***CLK12_CTL***	
(N.B: CLK48_CTL.div_clk48_pd must be set to '0' for clk12 functional clock to work)				
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:1	R/W	0h	sel_clk12	10 = sel_ext_clk12 - clk12 = SSI_TX 01 = exit_rst_clk12 - clk12 = functional clock 00 = clk12 = 27MHz xtal_clk
0	R/W	1	en_clk12	1 = enable clk12
Offset 0x04 7234			***CLK_IIC1_CTL***	
(N.B: CLK48_CTL.div_clk48_pd must be set to '0' for clk_iic1 functional clock to work)				
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:1	R/W	0h	sel_clk_iic1	10 = sel_ext_clk_iic1 - clk_iic1 = SSI_TX 01 = exit_rst_clk_iic1 - clk_iic1 = functional clock 00 = clk_iic1 = 27MHz xtal_clk
0	R/W	1	en_clk_iic1	1 = enable clk_iic1
Offset 0x04 7238			***CLK_IIC2_CTL***	
(N.B: CLK48_CTL.div_clk48_pd must be set to '0' for clk_iic2 functional clock to work)				
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:1	R/W	0h	sel_clk_iic2	10 = sel_ext_clk_iic2 - clk_iic2 = SSI_TX 01 = exit_rst_clk_iic2 - clk_iic2 = functional clock 00 = clk_iic2 = 27MHz xtal_clk
0	R/W	1	en_clk_iic2	1 = enable clk_iic2

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CLOCK REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x04 723C			***CLK_UART1_CTL***	
(N.B: CLK48_CTL.div_clk48_pd must be set to '0' for clk_uart1 functional clock to work)				
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:1	R/W	0h	sel_clk_uart1	10 = sel_ext_clk_uart1 - clk_uart1 = SSI_RXD 01 = exit_rst_clk_uart1 - clk_uart1 = functional clock 00 = clk_uart1 = 27MHz xtal_clk
0	R/W	1	en_clk_uart1	1 = enable clk_uart1
Offset 0x04 7240			***CLK_UART2_CTL***	
(N.B: CLK48_CTL.div_clk48_pd must be set to '0' for clk_uart2 functional clock to work)				
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:1	R/W	0h	sel_clk_uart2	10 = sel_ext_clk_uart2 - clk_uart2 = SSI_RXD 01 = exit_rst_clk_uart2 - clk_uart2 = functional clock 00 = clk_ uart2 = 27MHz xtal_clk
0	R/W	1	en_clk_uart2	1 = enable clk_uart2
Offset 0x04 7244			***CLK_UART3_CTL***	
(N.B: CLK48_CTL.div_clk48_pd must be set to '0' for clk_uart3 functional clock to work)				
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:1	R/W	0h	sel_clk_ uart3	10 = sel_ext_clk_ uart3 - clk_ uart3 = SSI_RXD 01 = exit_rst_clk_ uart3 - clk_ uart3 = functional clock 00 = clk_ uart3 = 27MHz xtal_clk
0	R/W	1	en_clk_uart3	1 = enable clk_uart3
Offset 0x04 7248			***MSP1_IN_CLK_SRC_CTL***	
31:20	R/W	n/a	Reserved	Read as 0, write nothing
19:16	R/W	0h	sel_msp1_in_clk_src2	1001 = select clock specified by bits [9:8] 0110 = select 1394rx_clk 0101 = select ts_p22_clk 0100 = select ts_p21_clk 0011 = select ts_p12_clk 0010 = select ts_p11_clk 0001 = select DV3_clk 0000 = select DV2_clk
15:10	R/W	n/a	Reserved	Read as 0, write nothing
9:8	R/W	0h	sel_msp1_in_clk_src	11 = select clock specified by bits [2:0] 10 = select dds8_clk_tsdma 01 = select DV3_clk 00 = select DV2_clk
7:3	R/W	n/a	Reserved	Read as 0, write nothing

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CLOCK REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
2:0	R/W	0h	sel_msp1_in_clk_div8	101 = select dds8_clk_option to be divided by 8 100 = select dds8_clk_tsdma to be divided by 8 011 = select ts_s22_clk to be divided by 8 010 = select DV3_clk to be divided by 8 001 = select ts_s12_clk to be divided by 8 000 = select DV2_clk to be divided by 8
Offset 0x04 724C			***MSP1_IN_CLK_CTL***	
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:1	R/W	0h	sel_msp1_in_clk_4x1mux	10 = sel_ext_clk_msp1 - clk_msp1 = SSI_SCLK_CTSN 01 = exit_rst_clk_msp1 - clk_msp1 = functional clock 00 = clk_msp1 = 27MHz xtal_clk
0	R/W	1	en_msp1_in_clk	1 = enable clk_msp1
Offset 0x04 7250			***CLK_PCI_CTL***	
31:4	R/W	n/a	Reserved	Read as 0, write nothing
3	R/W	0h	div_clk_pci_pd	1 = powerdown clk_pci divider in the CAB
2:1	R/W	0h	sel_clk_pci	10 = sel_ext_clk_pci - clk_pci = GPIO[7] 01 = exit_rst_clk_pci - clk_pci = functional clock 00 = clk_pci = 27MHz xtal_clk
0	R/W	1	en_clk_pci	1 = enable clk_pci
Offset 0x04 7254			***CLK_MBS_CTL***	
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:1	R/W	0h	sel_clk_mbs	10 = sel_ext_clk_mbs - clk_mbs = GPIO[5] 01 = exit_rst_clk_mbs - clk_mbs = functional clock 00 = clk_mbs = 27MHz xtal_clk
0	R/W	1	en_clk_mbs	1 = enable clk_mbs
Offset 0x04 7258			***CLK_SPDI_CTL***	
31:7	R/W	n/a	Reserved	Read as 0, write nothing
6	R/W	0h	div_clk_spdi_pd	1 = powerdown clk_spdi divider in the CAB
5:3	R/W	0h	div_clk_spdi	000 = clk_spdi = 144MHz, from CAB 001 = clk_spdi = 72MHZ, div by 2 in wsg_clock
2:1	R/W	0h	sel_clk_spdi	10 = sel_ext_clk_spdi - clk_spdi = UA2_TX 01 = exit_rst_clk_spdi - clk_spdi = functional clock 00 = clk_spdi = 27MHz xtal_clk
0	R/W	1	en_clk_spdi	1 = enable clk_spdi
Offset 0x04 725C			***CLK_TSTAMP_CTL***	
31:4	R/W	n/a	Reserved	Read as 0, write nothing
3	R/W	0	div_clk_tstamp_pd	1 = powerdown clk_tstamp divider in the CAB

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CLOCK REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
2:1	R/W	0h	sel_clk_tstamp	10 = sel_ext_clk_tstamp - clk_tstamp = UA1_RX 01 = exit_rst_clk_tstamp - clk_tstamp = functional clock 00 = clk_tstamp = 27MHz xtal_clk
0	R/W	1	en_clk_tstamp	1 = enable clk_tstamp
Offset 0x04 7260			***CLK_SPY_CTL***	
(N.B: CLK_TSTAMP_CTL.div_clk_tstamp_pd must be set to '0' for clk_spy functional clock to work)				
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:1	R/W	0h	sel_clk_spy	10 = sel_ext_clk_spy - clk_spy = SSI_FS_RTSN 01 = exit_rst_clk_spy - clk_spy = functional clock 00 = clk_spy = 27MHz xtal_clk
0	R/W	1	en_clk_spy	1 = enable clk_spy
Offset 0x04 7264			***CLK50_CTL (also controls CLK25 since they must be switched simultaneously)***	
31:2	R/W	n/a	Reserved	Read as 0, write nothing
1	R/W	1	exit_rst_clk50	0 = clk50 = 27MHz xtal_clk 1 = clk50 = functional clock
0	R/W	1	en_clk50	1 = enable clk50
Offset 0x04 7268			***CLK_VMSP1_CTL***	
(N.B: CLK_TSTAMP_CTL.div_clk_tstamp_pd must be set to '0' for clk_vmsp1 functional clock to work)				
31:4	R/W	n/a	Reserved	Read as 0, write nothing
3	R/W	0h	sel_invert_clk_vmsp1	1 = select inverted functional clock
2:1	R/W	0h	sel_clk_vmsp1	10 = sel_ext_clk_vmsp1 - clk_vmsp1 = UA1_RX 01 = exit_rst_clk_vmsp1 - clk_vmsp1 = functional clock 00 = clk_vmsp1 = 27MHz xtal_clk
0	R/W	1	en_clk_vmsp1	1 = enable clk_vmsp1
Offset 0x04 726C			***CLK_VMSP2_CTL***	
(N.B: CLK_TSTAMP_CTL.div_clk_tstamp_pd must be set to '0' for clk_vmsp2 functional clock to work)				
31:4	R/W	n/a	Reserved	Read as 0, write nothing
3	R/W	0h	sel_invert_clk_vmsp2	1 = select inverted functional clock
2:1	R/W	0h	sel_clk_vmsp2	10 = sel_ext_clk_vmsp2 - clk_vmsp2 = UA1_RX 01 = exit_rst_clk_vmsp2 - clk_vmsp2 = functional clock 00 = clk_vmsp2 = 27MHz xtal_clk
0	R/W	1	en_clk_vmsp2	1 = enable clk_vmsp2
Offset 0x04 7270			***CLK_NDS1_CTL***	
31:4	R/W	n/a	Reserved	Read as 0, write nothing
3	R/W	0h	sel_invert_clk_nds1	1 = select inverted functional clock
2:1	R/W	0h	sel_clk_nds1	10 = sel_ext_clk_nds1 - clk_nds1 = AIO_OSCLK 01 = exit_rst_clk_nds1 - clk_nds1 = functional clock 00 = clk_nds1 = 27MHz xtal_clk

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CLOCK REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
0	R/W	1	en_clk_nds1	1 = enable clk_nds1
Offset 0x04 7274			***CLK_NDS2_CTL***	
31:4	R/W	n/a	Reserved	Read as 0, write nothing
3	R/W	0h	sel_invert_clk_nds2	1 = select inverted functional clock
2:1	R/W	0h	sel_clk_nds2	10 = sel_ext_clk_nds2 - clk_nds2 = AIO_OSCLK 01 = exit_rst_clk_nds2 - clk_nds2 = functional clock 00 = clk_nds2 = 27MHz xtal_clk
0	R/W	1	en_clk_nds2	1 = enable clk_nds2
Offset 0x04 7278			***CLK_1394TX1_SRC_CTL***	
31:20	R/W	n/a	Reserved	Read as 0, write nothing
19:16	R/W	0h	sel_clk_1394tx1_src2	1001 = select clock specified by bits [9:8] 0111 = select mspout2_clk 0110 = select clk_tsdma 0101 = select ts_p22_clk 0100 = select ts_p21_clk 0011 = select ts_p12_clk 0010 = select ts_p11_clk 0001 = select DV3_clk 0000 = select DV2_clk
15:10	R/W	n/a	Reserved	Read as 0, write nothing
9:8	R/W	0h	sel_clk_1394tx1_src	11 = select clock divided by 8 (parallelization) 10 = select dds8_clk_tsdma 01 = select DV3_clk 00 = select DV2_clk
7:3	R/W	n/a	Reserved	Read as 0, write nothing
2:0	R/W	0h	sel_clk_1394tx1_div8	101 = select clk_option to be divided by 8 100 = select dds8_clk_tsdma to be divided by 8 011 = select ts_s22_clk to be divided by 8 010 = select DV3_clk to be divided by 8 001 = select ts_s12_clk to be divided by 8 000 = select DV2_clk to be divided by 8
Offset 0x04 727C			***CLK_1394TX1_CTL***	
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:1	R/W	0h	sel_clk_1394tx1_4x1mux	10 = sel_ext_clk_1394tx1 - clk_1394tx1 = SSI_SCLK_CTSN 01 = exit_rst_clk_1394tx1 - clk_1394tx1 = functional clock 00 = clk_1394tx1 = 27MHz xtal_clk
0	R/W	1	en_clk_1394tx1	1 = enable clk_1394tx1
Offset 0x04 7280			***CLK_1394TX2__SRC_CTL***	
31:20	R/W	n/a	Reserved	Read as 0, write nothing

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CLOCK REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
19:16	R/W	0h	sel_clk_1394tx2_src2	1001 = select clock specified by bits [9:8] 0111 = select mspout2_clk 0110 = select clk_tsdma 0101 = select ts_p22_clk 0100 = select ts_p21_clk 0011 = select ts_p12_clk 0010 = select ts_p11_clk 0001 = select DV3_clk 0000 = select DV2_clk
15:10	R/W	n/a	Reserved	Read as 0, write nothing
9:8	R/W	0h	sel_clk_1394tx2_src	11 = select clock divided by 8 (parallelization) 10 = select dds8_clk_tsdma 01 = select DV3_clk 00 = select DV2_clk
7:3	R/W	n/a	Reserved	Read as 0, write nothing
2:0	R/W	0h	sel_clk_1394tx2_div8	101 = select clk_option to be divided by 8 100 = select dds8_clk_tsdma to be divided by 8 011 = select ts_s22_clk to be divided by 8 010 = select DV3_clk to be divided by 8 001 = select ts_s12_clk to be divided by 8 000 = select DV2_clk to be divided by 8
Offset 0x04 7284			***CLK_1394TX2_CTL***	
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:1	R/W	0h	sel_clk_1394tx2_4x1mux	10 = sel_ext_clk_1394tx2 - clk_1394tx2 = SSI_SCLK_CTSN 01 = exit_rst_clk_1394tx2 - clk_1394tx2 = functional clock 00 = clk_1394tx2 = 27MHz xtal_clk
0	R/W	1	en_clk_1394tx2	1 = enable clk_1394tx2
Offset 0x04 7288			***CLK_TSDMA_SRC_CTL***	
31:10	R/W	n/a	Reserved	Read as 0, write nothing
9:8	R/W	0h	sel_clk_tsdma_src	11 = select clock divided by 8 (parallelization) 10 = select dds8_clk_tsdma 01 = select DV3_clk 00 = select DV2_clk
7:3	R/W	n/a	Reserved	Read as 0, write nothing
2:0	R/W	0h	sel_clk_tsdma_div8	101 = select clk_option to be divided by 8 100 = select dds8_clk_tsdma to be divided by 8 011 = select ts_s22_clk to be divided by 8 010 = select DV3_clk to be divided by 8 001 = select ts_s12_clk to be divided by 8 000 = select DV2_clk to be divided by 8

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CLOCK REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x04 728C			***CLK_TSDMA_CTL***	
31:4	R/W	n/a	Reserved	Read as 0, write nothing
3	R/W	0h	sel_invert_clk_tsdma	1 = select inverted functional clock
2:1	R/W	0h	sel_clk_tsdma_4x1mux	10 = sel_ext_clk_tsdma - clk_tsdma = SSI_SCLK_CTSN 01 = exit_rst_clk_tsdma - clk_tsdma = functional clock 00 = clk_tsdma = 27MHz xtal_clk
0	R/W	1	en_clk_tsdma	1 = enable clk_tsdma
Offset 0x04 7290			***TSOUT_CLK_OUT_SRC_CTL***	
31:4	R/W	n/a	Reserved	Read as 0, write nothing
3:0	R/W	0h	sel_tsout_clk_out_src	1000 = select dds8_clk_tsdma 0111 = select clk_tsdma 0110 = select mspout1_clk 0101 = select mspout2_clk 0100 = select 1394rx_clk 0011 = select ts_s22_clk 0010 = select DV3_clk 0001 = select ts_s12_clk 0000 = select DV2_clk
Offset 0x04 7294			***TSOUT_CLK_OUT_CTL***	
31:4	R/W	n/a	Reserved	Read as 0, write nothing
3	R/W	0h	sel_invert_tsout_clk_out	1 = select inverted functional clock
2:1	R/W	0h	sel_tsout_clk_out_4x1mux	10 = sel_ext_tsout_clk_out - tsout_clk_out = AIO_OSCLK 01 = exit_rst_tsout_clk_out - tsout_clk_out = functional clock 00 = tsout_clk_out = 27MHz xtal_clk
0	R/W	1	en_tsout_clk_out	1 = enable tsout_clk_out
Offset 0x04 7298			***TSOUT_SERIAL_CLK_CTL***	
31:4	R/W	n/a	Reserved	Read as 0, write nothing
3	R/W	0h	sel_invert_tsout_seial_clk	1 = select inverted functional clock
2:1	R/W	0h	sel_tsout_serial_clk	10 = sel_ext_tsout_serial_clk - tsout_serial_clk = AIO_OSCLK 01 = exit_rst_tsout_serial_clk - tsout_serial_clk = functional clock 00 = tsout_serial_clk = 27MHz xtal_clk
0	R/W	1	en_tsout_serial_clk	1 = enable tsout_serial_clk
Offset 0x04 729C			***RESERVED***	
Offset 0x04 7300			***CLK_ICP1_MUX_CTL***	
31:4	R/W	n/a	Reserved	Read as 0, write nothing
3	R/W	0h	sel_invert_clk_icp1_mux	1 = select inverted functional clock
2:1	R/W	0h	sel_clk_icp1_mux	10 = sel_ext_clk_icp1_mux - clk_icp1_mux = UA2_RX 01 = exit_rst_clk_icp1_mux - clk_icp1_mux = functional clock 00 = clk_icp1_mux = 27MHz xtal_clk

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CLOCK REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
0	R/W	1	en_clk_icp1_mux	1 = enable clk_icp1_mux
Offset 0x04 7304			***CLK_ICP1_CTL***	
31:7	R/W	n/a	Reserved	Read as 0, write nothing
6	R/W	0	sel_invert_clk_icp1	1 = select inverted clock from divider
5:3	R/W	1	div_clk_icp1	Divide clk_icp1: 101 = divide clock by 8 100 = divide clock by 6 011 = divide clock by 4 010 = divide clock by 3 001 = divide clock by 2 000 = no divide
2:1	R/W	0h	sel_clk_icp1	10 = sel_ext_clk_icp1 - clk_icp1 = UA2_RTSN 01 = exit_rst_clk_icp1 - clk_icp1 = functional clock 00 = clk_icp1 = 27MHz xtal_clk
0	R/W	1	en_clk_icp1	1 = enable clk_icp1
Offset 0x04 7308			***CLK_ICP2_MUX_CTL***	
31:4	R/W	n/a	Reserved	Read as 0, write nothing
3	R/W	0h	sel_invert_clk_icp2_mux	1 = select inverted functional clock
2:1	R/W	0h	sel_clk_icp2_mux	10 = sel_ext_clk_icp2_mux - clk_icp2_mux = UA2_RX 01 = exit_rst_clk_icp2_mux - clk_icp2_mux = functional clock 00 = clk_icp2_mux = 27MHz xtal_clk
0	R/W	1	en_clk_icp2_mux	1 = enable clk_icp2_mux
Offset 0x04 730C			***CLK_ICP2_CTL***	
31:7	R/W	n/a	Reserved	Read as 0, write nothing
6	R/W	0	sel_invert_clk_icp2	1 = select inverted clock from divider
5:3	R/W	1	div_clk_icp2	Divide clk_icp1: 101 = divide clock by 8 100 = divide clock by 6 011 = divide clock by 4 010 = divide clock by 3 001 = divide clock by 2 000 = no divide
2:1	R/W	0h	sel_clk_icp2	10 = sel_ext_clk_icp2 - clk_icp2 = UA2_RTSN 01 = exit_rst_clk_icp2 - clk_icp2 = functional clock 00 = clk_icp2 = 27MHz xtal_clk
0	R/W	1	en_clk_icp2	1 = enable clk_icp2
Offset 0x04 7310			***AI1_OSCLK_CTL***	
31:3	R/W	n/a	Reserved	Read as 0, write nothing

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CLOCK REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
2:1	R/W	0h	sel_ai1_osclk	10 = sel_ext_ai1_osclk - ai1_osclk = UA2_CTSN 01 = exit_rst_ai1_osclk - ai1_osclk = functional clock 00 = ai1_osclk = 27MHz xtal_clk
0	R/W	1	en_ai1_osclk	1 = enable ai1_osclk
Offset 0x04 7314			***AO1_OSCLK_CTL***	
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:1	R/W	0h	sel_ao1_osclk	10 = sel_ext_ao1_osclk - ao1_osclk = UA2_CTSN 01 = exit_rst_ao1_osclk - ao1_osclk = functional clock 00 = ao1_osclk = 27MHz xtal_clk
0	R/W	1	en_ao1_osclk	1 = enable ao1_osclk
Offset 0x04 7318			***AI2_OSCLK_CTL***	
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:1	R/W	0h	sel_ai2_osclk	10 = sel_ext_ai2_osclk - ai2_osclk = UA2_CTSN 01 = exit_rst_ai2_osclk - ai2_osclk = functional clock 00 = ai2_osclk = 27MHz xtal_clk
0	R/W	1	en_ai2_osclk	1 = enable ai2_osclk
Offset 0x04 731C			***AO2_OSCLK_CTL***	
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:1	R/W	0h	sel_ao2_osclk	10 = sel_ext_ao2_osclk - ao2_osclk = UA2_CTSN 01 = exit_rst_ao2_osclk - ao2_osclk = functional clock 00 = ao2_osclk = 27MHz xtal_clk
0	R/W	1	en_ao2_osclk	1 = enable ao2_osclk
Offset 0x04 7320			***AIO3_OSCLK_CTL***	
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:1	R/W	0h	sel_aio3_osclk	10 = sel_ext_aio3_osclk - aio3_osclk = UA2_CTSN 01 = exit_rst_aio3_osclk - aio3_osclk = functional clock 00 = aio3_osclk = 27MHz xtal_clk
0	R/W	1	en_aio3_osclk	1 = enable aio3_osclk
Offset 0x04 7324			***CLK_SPDO_CTL***	
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:1	R/W	0h	sel_clk_spdo	10 = sel_ext_clk_spdo - clk_spdo = UA1_RX 01 = exit_rst_clk_spdo - clk_spdo = functional clock 00 = clk_spdo = 27MHz xtal_clk
0	R/W	1	en_clk_spdo	1 = enable clk_spdo
Offset 0x04 7328—739C			***RESERVED***	
Offset 0x04 7400			***GPIO_CLK_Q0_CTL***	
31:2	R/W	n/a	Reserved	Read as 0, write nothing

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CLOCK REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
1	R/W	0	exit_rst_gpio_clkout_q0	0 = gpio_clkout_q0 = 27MHz xtal_clk 1 = gpio_clkout_q0 = functional clock
0	R/W	1	en_gpio_clkout_q0	1 = enable gpio_clkout_q0
Offset 0x04 7404			***GPIO_CLK_Q1_CTL***	
31:2	R/W	n/a	Reserved	Read as 0, write nothing
1	R/W	0	exit_rst_gpio_clkout_q1	0 = gpio_clkout_q1 = 27MHz xtal_clk 1 = gpio_clkout_q1 = functional clock
0	R/W	1	en_gpio_clkout_q1	1 = enable gpio_clkout_q1
Offset 0x04 7408			***GPIO_CLK_Q2_CTL***	
31:2	R/W	n/a	Reserved	Read as 0, write nothing
1	R/W	0	exit_rst_gpio_clkout_q2	0 = gpio_clkout_q2 = 27MHz xtal_clk 1 = gpio_clkout_q2 = functional clock
0	R/W	1	en_gpio_clkout_q2	1 = enable gpio_clkout_q2
Offset 0x04 740C			***GPIO_CLK_Q3_CTL***	
31:2	R/W	n/a	Reserved	Read as 0, write nothing
1	R/W	0	exit_rst_gpio_clkout_q3	0 = gpio_clkout_q3 = 27MHz xtal_clk 1 = gpio_clkout_q3 = functional clock
0	R/W	1	en_gpio_clkout_q3	1 = enable gpio_clkout_q3
Offset 0x04 7410—741C			***Reserved***	
Offset 0x04 7420			***CLK_VIP1_SEL_CTL***	
(NB: VIP1 data muxing must be programmed in the IO-MUX to match the programming of the VIP1 clock muxing)				
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:0	R/W	0h	sel_clk_vip1_src	100 = source is clk_1394rx 011 = source is clk_icp_out2 010 = source is DV3_CLK pad 001 = source is DV2_CLK pad 000 = source is DV1_CLK pad
Offset 0x04 7424			***CLK_VIP2_SEL_CTL***	
(NB: VIP2 data muxing must be programmed in the IO-MUX to match the programming of the VIP2 clock muxing)				
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:0	R/W	0h	sel_clk_vip2_src	100 = source is clk_1394rx 011 = source is clk_icp_out1 010 = source is DV3_CLK pad 001 = source is DV2_CLK pad 000 = source is DV1_CLK pad
Offset 0x04 7428			***CLK_SMART2_CTL***	
(N.B: CLK_TSTAMP_CTL.div_clk_tstamp_pd must be set to ‘0’ for clk_smart2 functional clock to work)				
31:3	R/W	n/a	Reserved	Read as 0, write nothing

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CLOCK REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
2:1	R/W	0	sel_clk_smart2	10 = sel_ext_clk_clk_smart2: clk_smart2 = ext clock 01 = exit_rst_clk_smart2: clk_smart2 = functional clock 00 = clk_smart2 = 27MHz xtal_clk
0	R/W	1	en_clk_smart2	1 = enable clk_smart2
Offset 0x04 742C			***CLK_AI1_SCK_O_CTL***	
31:2	R/W	n/a	Reserved	Read as 0, write nothing
1	R/W	0	exit_rst_clk_ai1_sck_o	0 = clk_ai1_sck_o = 27MHz xtal_clk 1 = clk_ai1_sck_o = functional clock
0	R/W	1	en_clk_ai1_sck_o	1 = enable clk_ai1_sck_o
Offset 0x04 7430			***CLK_AO1_SCK_O_CTL***	
31:2	R/W	n/a	Reserved	Read as 0, write nothing
1	R/W	0	exit_rst_clk_ao1_sck_o	0 = clk_ao1_sck_o = 27MHz xtal_clk 1 = clk_ao1_sck_o = functional clock
0	R/W	1	en_clk_ao1_sck_o	1 = enable clk_ao1_sck_o
Offset 0x04 7434			***CLK_AI2_SCK_O_CTL***	
31:2	R/W	n/a	Reserved	Read as 0, write nothing
1	R/W	0	exit_rst_clk_ai2_sck_o	0 = clk_ai2_sck_o = 27MHz xtal_clk 1 = clk_ai2_sck_o = functional clock
0	R/W	1	en_clk_ai2_sck_o	1 = enable clk_ai2_sck_o
Offset 0x04 7438			***CLK_AO2_SCK_O_CTL***	
31:2	R/W	n/a	Reserved	Read as 0, write nothing
1	R/W	0	exit_rst_clk_ao2_sck_o	0 = clk_ao2_sck_o = 27MHz xtal_clk 1 = clk_ao2_sck_o = functional clock
0	R/W	1	en_clk_ao2_sck_o	1 = enable clk_ao2_sck_o
Offset 0x04 743C			***CLK_AIO3_SCK_O_CTL***	
31:2	R/W	n/a	Reserved	Read as 0, write nothing
1	R/W	0	exit_rst_clk_aio3_sck_o	0 = clk_aio3_sck_o = 27MHz xtal_clk 1 = clk_aio3_sck_o = functional clock
0	R/W	1	en_clk_aio3_sck_o	1 = enable clk_aio3_sck_o
Offset 0x04 7440—745C			***RESERVED***	
Offset 0x04 7460			***CLK_OPTION_CTL***	
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:0	R/W	0	sel_clk_option_div	101 = divide clock by 8: 2.25MHz 100 = divide clock by 6: 3.0MHz 011 = divide clock by 4: 4.5MHz 010 = divide clock by 3: 6MHz 001 = divide clock by 2: 9MHz 000 = no divide: 18MHz

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CLOCK REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x04 7464			***MSPOUT1_CLK_SRC_CTL***	
31:10	R/W	n/a	Reserved	Read as 0, write nothing
9:8	R/W	0h	sel_mspout1_clk_src	11 = select clock divided by 8 (parallelization) 10 = select dds8_clk_tsdma 01 = select DV3_clk 00 = select DV2_clk
7:3	R/W	n/a	Reserved	Read as 0, write nothing
2:0	R/W	0h	sel_mspout1_clk_div8	101 = select clk_option to be divided by 8 100 = select dds8_clk_tsdma to be divided by 8 011 = select ts_s22_clk to be divided by 8 010 = select DV3_clk to be divided by 8 001 = select ts_s12_clk to be divided by 8 000 = select DV2_clk to be divided by 8
Offset 0x04 7468			***MSPOUT1_CLK_CTL***	
31:4	R/W	n/a	Reserved	Read as 0, write nothing
3	R/W	0h	sel_invert_mspout1_clk	1 = select inverted functional clock
2:1	R/W	0h	sel_mspout1_clk_4x1mux	10 = sel_ext_mspout1_clk - mspout1_clk = SSI_SCLK_CTSN 01 = exit_rst_mspout1_clk - mspout1_clk = functional clock 00 = mspout1_clk = 27MHz xtal_clk
0	R/W	1	en_mspout1_clk	1 = enable mspout1_clk
Offset 0x04 746C			***MSPOUT2_CLK_SRC_CTL***	
31:10	R/W	n/a	Reserved	Read as 0, write nothing
9:8	R/W	0h	sel_mspout2_clk_src	11 = select clock divided by 8 (parallelization) 10 = select dds8_clk_tsdma 01 = select DV3_clk 00 = select DV2_clk
7:3	R/W	n/a	Reserved	Read as 0, write nothing
2:0	R/W	0h	sel_mspout2_clk_div8	101 = select clk_option to be divided by 8 100 = select dds8_clk_tsdma to be divided by 8 011 = select ts_s22_clk to be divided by 8 010 = select DV3_clk to be divided by 8 001 = select ts_s12_clk to be divided by 8 000 = select DV2_clk to be divided by 8
Offset 0x04 7470			***MSPOUT2_CLK_CTL***	
31:4	R/W	n/a	Reserved	Read as 0, write nothing
3	R/W	0h	sel_invert_mspout2_clk	1 = select inverted functional clock
2:1	R/W	0h	sel_mspout2_clk_4x1mux	10 = sel_ext_mspout2_clk - mspout2_clk = SSI_SCLK_CTSN 01 = exit_rst_mspout2_clk - mspout2_clk = functional clock 00 = mspout2_clk = 27MHz xtal_clk

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CLOCK REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
0	R/W	1	en_mspout2_clk	1 = enable mspout2_clk
Offset 0x04 7474			***CLK_1394RX_SRC_CTL***	
31:10	R/W	n/a	Reserved	Read as 0, write nothing
9:8	R/W	0h	sel_clk_1394rx_src	11 = select clock divided by 8 (parallelization) 10 = select dds8_clk_tsdma 01 = select DV3_clk 00 = select DV2_clk
7:3	R/W	n/a	Reserved	Read as 0, write nothing
2:0	R/W	0h	sel_clk_1394rx_div8	101 = select clk_option to be divided by 8 100 = select dds8_clk_tsdma to be divided by 8 011 = select ts_s22_clk to be divided by 8 010 = select DV3_clk to be divided by 8 001 = select ts_s12_clk to be divided by 8 000 = select DV2_clk to be divided by 8
Offset 0x04 7478			***CLK_1394RX_CTL***	
31:4	R/W	n/a	Reserved	Read as 0, write nothing
3	R/W	0h	sel_invert_1394rx_clk	1 = select inverted functional clock
2:1	R/W	0h	sel_clk_1394rx_4x1mux	10 = sel_ext_clk_1394rx - clk_1394rx = SSI_SCLK_CTSN 01 = exit_rst_clk_1394rx - clk_1394rx = functional clock 00 = clk_1394rx = 27MHz xtal_clk
0	R/W	1	en_clk_1394rx	1 = enable clk_1394rx
Offset 0x04 747C			***MSP2_IN_CLK_SRC_CTL***	
31:20	R/W	n/a	Reserved	Read as 0, write nothing
19:16	R/W	0h	sel_msp2_in_clk_src2	1001 = select clock specified by bits [9:8] 0110 = select 1394rx_clk 0101 = select ts_p22_clk 0100 = select ts_p21_clk 0011 = select ts_p12_clk 0010 = select ts_p11_clk 0001 = select DV3_clk 0000 = select DV2_clk
15:10	R/W	n/a	Reserved	Read as 0, write nothing
9:8	R/W	0h	sel_msp2_in_clk_src	11 = select clock divided by 8 (parallelization) 10 = select dds8_clk_tsdma 01 = select DV3_clk 00 = select DV2_clk
7:3	R/W	n/a	Reserved	Read as 0, write nothing

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CLOCK REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
2:0	R/W	0h	sel_msp2_in_clk_div8	101 = select dds8_clk_option to be divided by 8 100 = select dds8_clk_tsdma to be divided by 8 011 = select ts_s22_clk to be divided by 8 010 = select DV3_clk to be divided by 8 001 = select ts_s12_clk to be divided by 8 000 = select DV2_clk to be divided by 8
Offset 0x04 7480			***MSP2_IN_CLK_CTL***	
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:1	R/W	0h	sel_msp2_in_clk_4x1mux	10 = sel_ext_clk_msp2 - clk_msp2 = SSI_SCLK_CTSN 01 = exit_rst_clk_msp2 - clk_msp2 = functional clock 00 = clk_msp2 = 27MHz xtal_clk
0	R/W	1	en_msp2_in_clk	1 = enable clk_msp2
Offset 0x04 7484			***TSOUT_PARALLEL_CLK_SRC_CTL***	
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:0	R/W	0h	sel_tsout_parallel_clk_src	110 = select parallel clock (divided by 8) 101 = select clk_tsdma 100 = select mspout1_clk 011 = select mspout2_clk 010 = select 1394rx_clk 001 = select DV3_clk 000 = select DV2_clk
Offset 0x04 7488			***TSOUT_PARALLEL_CLK_CTL***	
31:4	R/W	n/a	Reserved	Read as 0, write nothing
3	R/W	0h	sel_invert_tsout_parallel_clk	1 = select inverted functional clock
2:1	R/W	0h	sel_tsout_parallel_clk_4x1mux	10 = sel_ext_tsout_parallel_clk - tsout_parallel_clk = AIO_WS 01 = exit_rst_tsout_parallel_clk - tsout_parallel_clk = functional clock 00 = tsout_parallel_clk = 27MHz xtal_clk
0	R/W	0	en_tsout_parallel_clk	1 = enable tsout_parallel_clk
Offset 0x04 748C			***CLK_VMSP3_CTL***	
(N.B: CLK_TSTAMP_CTL.div_clk_tstamp_pd must be set to '0' for clk_vmsp3 functional clock to work)				
31:4	R/W	n/a	Reserved	Read as 0, write nothing
3	R/W	0h	sel_invert_clk_vmsp3	1 = select inverted functional clock
2:1	R/W	0h	sel_clk_vmsp3	10 = sel_ext_clk_vmsp3 - clk_vmsp1 = UA1_RX 01 = exit_rst_clk_vmsp3 - clk_vmsp1 = functional clock 00 = clk_vmsp3 = 27MHz xtal_clk
0	R/W	1	en_clk_vmsp3	1 = enable clk_vmsp3
Offset 0x04 7490			***MSP3_IN_CLK_SRC_CTL***	
31:20	R/W	n/a	Reserved	Read as 0, write nothing

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CLOCK REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
19:16	R/W	0h	sel_msp3_in_clk_src2	1001 = select clock specified by bits [9:8] 0110 = select 1394rx_clk 0101 = select ts_p22_clk 0100 = select ts_p21_clk 0011 = select ts_p12_clk 0010 = select ts_p11_clk 0001 = select DV3_clk 0000 = select DV2_clk
15:10	R/W	n/a	Reserved	Read as 0, write nothing
9:8	R/W	0h	sel_msp3_in_clk_src	11 = select clock divided by 8 (parallelization) 10 = select dds8_clk_tsdma 01 = select DV3_clk 00 = select DV2_clk
7:3	R/W	n/a	Reserved	Read as 0, write nothing
2:0	R/W	0h	sel_msp3_in_clk_div8	101 = select dds8_clk_option to be divided by 8 100 = select dds8_clk_tsdma to be divided by 8 011 = select ts_s22_clk to be divided by 8 010 = select DV3_clk to be divided by 8 001 = select ts_s12_clk to be divided by 8 000 = select DV2_clk to be divided by 8
Offset 0x04 7494			***MSP3_IN_CLK_CTL***	
31:3	R/W	n/a	Reserved	Read as 0, write nothing
2:1	R/W	0h	sel_msp3_in_clk_4x1mux	10 = sel_ext_clk_msp3 - clk_msp3 = SSI_SCLK_CTSN 01 = exit_rst_clk_msp3 - clk_msp3 = functional clock 00 = clk_msp3 = 27MHz xtal_clk
0	R/W	1	en_msp3_in_clk	1 = enable clk_msp2
Offset 0x04 7498			***MSPOUT3_CLK_SRC_CTL***	
31:10	R/W	n/a	Reserved	Read as 0, write nothing
9:8	R/W	0h	sel_mspout3_clk_src	11 = select clock divided by 8 (parallelization) 10 = select dds8_clk_tsdma 01 = select DV3_clk 00 = select DV2_clk
7:3	R/W	n/a	Reserved	Read as 0, write nothing
2:0	R/W	0h	sel_mspout3_clk_div8	101 = select clk_option to be divided by 8 100 = select dds8_clk_tsdma to be divided by 8 011 = select ts_s22_clk to be divided by 8 010 = select DV3_clk to be divided by 8 001 = select ts_s12_clk to be divided by 8 000 = select DV2_clk to be divided by 8
Offset 0x04 749C			***MSPOUT3_CLK_CTL***	

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CLOCK REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
31:4	R/W	n/a	Reserved	Read as 0, write nothing
3	R/W	0h	sel_invert_mspout3_clk	1 = select inverted functional clock
2:1	R/W	0h	sel_mspout3_clk_4x1mux	10 = sel_ext_mspout3_clk - mspout3_clk = SSI_SCLK_CTSN 01 = exit_rst_mspout3_clk - mspout3_clk = functional clock 00 = mspout3_clk = 27MHz xtal_clk
0	R/W	1	en_mspout3_clk	1 = enable mspout3_clk
Offset 0x04 74A0—7FF8			*RESERVED*	
Offset 0x04 7FE0			*INTERRUPT STATUS*	
31	R	0	ts_s22_clk_present	1 = Clock present 0 = Clock NOT present
30	R	0	ts_s12_clk_present	1 = Clock present 0 = Clock NOT present
29	R	0	aio3_sckin_present	1 = Clock present 0 = Clock NOT present
28	R	0	ai2_sckin_present	1 = Clock present 0 = Clock NOT present
27	R	0	ai1_sckin_present	1 = Clock present 0 = Clock NOT present
26	R	0	clk_1394_present	1 = Clock present 0 = Clock NOT present
25	R	0	dv3_clk_present	1 = Clock present 0 = Clock NOT present
24	R	0	dv2_clk_present	1 = Clock present 0 = Clock NOT present
23	R	0	dv1_clk_present	1 = Clock present 0 = Clock NOT present
22:9	R/W	n/a	Reserved	Read as 0, write nothing
8	R	0	ts_s22_clk_int	1 = Clock int
7	R	0	ts_s12_clk_int	1 = Clock int
6	R	0	aio3_sckin_int	1 = Clock int
5	R	0	ai2_sckin_int	1 = Clock int
4	R	0	ai1_sckin_int	1 = Clock int
3	R	0	clk_1394_int	1 = Clock int
2	R	0	dv3_clk_int	1 = Clock int
1	R	0	dv2_clk_int	1 = Clock int
0	R	0	dv1_clk_int	1 = Clock int
Offset 0x04 7FE4			*INTERRUPT ENABLE*	
31:9	R/W	n/a	Reserved	Read as 0, write nothing

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CLOCK REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
8	R/W	0	ts_s22_clk_int enable	1 = Interrupt enabled 0 = Interrupt NOT enabled
7	R/W	0	ts_s12_clk_int enable	1 = Interrupt enabled 0 = Interrupt NOT enabled
6	R/W	0	aio3_sckin_int enable	1 = Interrupt enabled 0 = Interrupt NOT enabled
5	R/W	0	ai2_sckin_int enable	1 = Interrupt enabled 0 = Interrupt NOT enabled
4	R/W	0	ai1_sckin_int enable	1 = Interrupt enabled 0 = Interrupt NOT enabled
3	R/W	0	clk_1394_int enable	1 = Interrupt enabled 0 = Interrupt NOT enabled
2	R/W	0	dv3_clk_int enable	1 = Interrupt enabled 0 = Interrupt NOT enabled
1	R/W	0	dv2_clk_int enable	1 = Interrupt enabled 0 = Interrupt NOT enabled
0	R/W	0	dv1_clk_int enable	1 = Interrupt enabled 0 = Interrupt NOT enabled
Offset 0x04 7FE8			***INTERRUPT CLEAR***	
31:9	R/W	n/a	Reserved	Read as 0, write nothing
8	R/W	0	clear ts_s22_clk_int	1 = clear interrupt
7	R/W	0	clear ts_s12_clk_int	1 = clear interrupt
6	R/W	0	clear aio3_sckin_int	1 = clear interrupt
5	R/W	0	clear ai2_sckin_int	1 = clear interrupt
4	R/W	0	clear ai1_sckin_int	1 = clear interrupt
3	R/W	0	clear clk_1394_int	1 = clear interrupt
2	R/W	0	clear dv3_clk_int	1 = clear interrupt
1	R/W	0	clear dv2_clk_int	1 = clear interrupt
0	R/W	0	clear dv1_clk_int	1 = clear interrupt
Offset 0x04 7FEC			***SET INTERRUPT***	
31:9	R/W	n/a	Reserved	Read as 0, write nothing
8	R/W	0	set ts_s22_clk_int	1 = set interrupt
7	R/W	0	set ts_s12_clk_int	1 = set interrupt
6	R/W	0	set aio3_sckin_int	1 = set interrupt
5	R/W	0	set ai2_sckin_int	1 = set interrupt
4	R/W	0	set ai1_sckin_int	1 = set interrupt
3	R/W	0	set clk_1394_int	1 = set interrupt

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CLOCK REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
2	R/W	0	set dv3_clk_int	1 = set interrupt
1	R/W	0	set dv2_clk_int	1 = set interrupt
0	R/W	0	set dv1_clk_int	1 = set interrupt
Offset 0x04 7FF0			***RESERVED***	
Offset 0x04 7FF4			***POWERDOWN***	
31	R/W	0	POWER_DOWN	Powerdown register for the module 0 = Normal operation of the peripheral. This is the reset value. 1 = Module is powered down and module clock can be removed. At powerdown, module responds to all reads with DEADABBA (except for reads of powerdown bit) and all writes with ERR ACK (except for writes to powerdown bit).
30:0		-	Unused	Ignore during writes and read as zeroes.
Offset 0x04 7FF8			***RESERVED***	
Offset 0x04 7FFC			***MODULE_ID***	
31:16	R	0x0108	module_id	Module ID
15:12	R	1	rev_major	Major revision
11:8	R	0	rev_minor	Minor revision
7:0	R	0	app_size	Aperture size is 0 = 4 kB.

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USB Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.13)

USB REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x04 8000			*HcRevision*	
31:8			Reserved	
7:0	R	10	Rev	Contains BCD value of the HCI specification implemented in PNX8526
Offset 0x04 8004			*HcControl*	
31:11			Reserved	
10	R/W	0b	RWE	Remote Wakeup Enable
9	R/W	0b	RWC	Remote Wakeup Connected. This bit is set during POST by system firmware to indicate the HC supports remote wakeup signaling. Bit is reset after a h/w reset but doesn't alter its value after a s/w reset.
8	R/W	0b	IR	Interrupt Routing 0 = All interrupts are routed to normal host bus interrupt mechanism. 1 = Interrupts are sent to SMI. (not used in Viper)
7:6	R/W	00b	HCFS	Host Controller Functional State for USB 00b = USB RESET 01b = USB RESUME 10b = USB OPERATIONAL 11b = USB SUSPEND The hardware may automatically transition from USB SUSPEND state to USB RESUME state. The hardware enters USB SUSPEND state after a software reset, where as it enters USB RESET after a hardware reset.
5	R/W	0b	BLE	Bulk List Enable
4	R/W	0b	CLE	Control List Enable
3	R/W	0b	IE	Isochronous Enable
2	R/W	0b	PLE	Periodic List Enable
1:0	R/W	00b	CBSR	Control Bulk Service Ratio
Offset 0x04 8008			*HcCommandStatus*	
31:18			Reserved	
17:16	R	00b	SOC	Scheduling Overrun Count These bits are incremented on each scheduling overrun error.
15:4			Reserved	
3	W	0b	OCR	Ownership Change Request. This bit is auto cleared after setting 0x000C[30].

USB REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
2	R/W	0b	BLF	Bulk List Filled This bit is set by s/w to indicate that there is a pending TD in the bulk list. This bit is cleared by h/w after servicing the TD.
1	R/W	0b	CLF	Control List Filled This bit is set by s/w to indicate that there is a pending TD in the control list. This bit is cleared by h/w after servicing the TD.
0	R/w	0b	HCR	Host Controller Reset This bit is set to initiate a s/w reset. The h/w moves into the USB SUSPEND state and resets all registers unless otherwise noted. This bit gets self cleared after the reset operation is over.
Offset 0x04 800C			*HcInterruptStatus**	
*These bits are automatically set by H/W and can be only cleared by writing a 1 to the corresponding bit.				
31			Reserved	
30	R/W	0b	OC	Ownership Change.
29:7		0b	Reserved	
6	R/W	0b	RHSC	Root Hub Status Change
5	R/W	0b	FNO	Frame Number Overflow
4	R/W	0b	UE	Unrecoverable Error
3	R/W	0b	RD	Resume Detected
2	R/W	0b	SF	Start of Frame
1	R/W	0b	WDH	Writeback Done Head
0	R/W	0b	SO	Scheduling Overrun
Offset 0x04 8010			*HcInterruptEnable**	
*These bits may be set by writing a 1. Writing 0 has no effect. Bits are cleared by writing a 1 to corresponding bit in register 0x04 8014.				
31	R/W	0b	MIE	0 = Ignore by HC 1 = Enable interrupt generation due to events specified in the other bits of this register. Used by HCD as a Master Interrupt Enable.
30	R/W	0b	OC	0 = Ignore 1 = Enable interrupt generation due to Ownership Change.
29:7		0b	Reserved	
6	R/W	0b	RHSC	0 = Ignore 1 = Enable interrupt generation due to Root Hub Status Change.
5	R/W	0b	FNO	0 = Ignore 1 = Enable interrupt generation due to Frame Number Overflow.
4	R/W	0b	UE	0 = Ignore 1 = Enable interrupt generation due to Unrecoverable Error.
3	R/W	0b	RD	0 = Ignore 1 = Enable interrupt generation due to Resume Detect.
2	R/W	0b	SF	0 = Ignore 1 = Enable interrupt generation due to Start of Frame.
1	R/W	0b	WDH	0 = Ignore 1 = Enable interrupt generation due to Hc Done Head Writeback.
0	R/W	0b	SO	0 = Ignore 1 = Enable interrupt generation due to Scheduling Overrun.

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USB REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x04 8014			*HcInterruptDisable**	
*This register reads back the contents of register 0x04 8010. Writing a 1 disables the corresponding interrupt bit by clearing the bit in register 0x04 8010.				
31	W	0b	MIE	0 = Ignore by HC 1 = Disable interrupt generation due to events specified in the other bits of this register. Used by HCD as a Master Interrupt Enable.
30	W	0b	OC	0 = Ignore 1 = Disable interrupt generation due to Ownership Change.
29:7		0b	Reserved	
6	W	0b	RHSC	0 = Ignore 1 = Disable interrupt generation due to Root Hub Status Change.
5	W	0b	FNO	0 = Ignore 1 = Disable interrupt generation due to Frame Number Overflow.
4	W	0b	UE	0 = Ignore 1 = Disable interrupt generation due to Unrecoverable Error.
3	W	0b	RD	0 = Ignore 1 = Disable interrupt generation due to Resume Detect.
2	W	0b	SF	0 = Ignore 1 = Disable interrupt generation due to Start of Frame.
1	W	0b	WDH	0 = Ignore 1 = Disable interrupt generation due to Hc Done Head Writeback.
0	W	0b	SO	0 = Ignore 1 = Disable interrupt generation due to Scheduling Overrun.
Offset 0x04 8018			*HcHCCA*	
31:8	R/W	0	HcHCCA	Base address of the Host Controller Communication Area.
7:0		-	Unused	
Offset 0x04 801C			*HcPCED*	
31:4	R	0	HcPCED	Period Current ED
3:0		-	Unused	
Offset 0x04 8020			*HcCHED*	
31:4	R/W	0	HcCHED	Control Head ED
3:0		-	Unused	
Offset 0x04 8024			*HcCCED*	
31:4	R/W	0	HcCCED	Control Current ED
3:0		-	Unused	
Offset 0x04 8028			*HcBHED*	
31:4	R/W	0	HcBHED	Bulk Head ED
3:0		-	Unused	
Offset 0x04 802C			*HcBCED*	
31:4	R/W	0	HcBCED	Bulk Current ED
3:0		-	Unused	
Offset 0x04 8030			*HcDH*	

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USB REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
31:4	R	0	HcDH	Done Head
3:0		-	Unused	
Offset 0x04 8034			*HcFMInterval*	
31	R/W	0b	FIT	Frame Interval Toggle
30:16	R/W	0	FSMPS	FS Largest Data Packet
15:14			Reserved	
13:0	R/W	2EDF	FI	Frame Interval
Offset 0x04 8038			*HcFMRemaining*	
31	R	0b	FRT	Frame Remaining Toggle
30:14			Reserved	
13:0	R	0	FR	Frame Remaining
Offset 0x04 803C			*HcFMNumber*	
31:16			Reserved	
15:0	R	0	FN	Frame Number
Offset 0x04 8040			*HcPeriodic Start*	
31:14			Reserved	
13:0	R/W	0	PS	Periodic Start
Offset 0x04 8044			*HcLSThreshold*	
31:12			Reserved	
11:0	R/W	0628	LST	LS Threshold
Offset 0x04 8048			*HcRHDescriptorA*	
31:24	R/W	02	POTPGT	Power On To Power Good Time
23:13		000	Reserved	
12	R/W	0	NOCP	No Over Current Protection
11	R/W	0	OCPM	Over Current Protection Mode
10	R	0	DT	DeviceType
9	R/W	0	NPS	No Power Switching
8	R/W	0	PSM	Power Switching Mode
7:0	R	02	NDP	Number Downstream Ports
Offset 0x04 804C			*HcRHDescriptorB*	
31:19	R	0	Reserved	Reserved
18:17	R/W	0	PPCM	Port Power Control Mask for port #2 & port #1
16:3	R	0	Reserved	Reserved
2:1	R/W	0		
0	R	0	Reserved	Reserved
Offset 0x04 8050			*HcRHStatus*	
31	W	0	CRWE	(W) ClearRemote Wakeup Enable. Writing a 1 clears the DRWE bit.
30:18			Reserved	

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USB REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
17	R/W	0b	CCIC	Over Current Indicator Change. Automatically set by h/w whenever there is a change in OCI bit. Cleared by writing a 1. Write 0 has no effect.
16	W	0b	LPSC	(R) Local Power Status Change. Always Read 0. (W) Set Global Power.
15	R/W	0b	DRWE	(R) Device Remote Wakeup Enable. 0 = Disabled 1 = Enabled (W) Set Remote Wakeup Enable by writing a 1. Write 0 has no effect.
14:2			Reserved	
1	R	0b	OCI	Over Current Indicator
0	W	0b	LPS	(R) Local Power Status. Always read 0 (W) 1 = Clear Global Power. 0 = No effect.
Offset 0x04 8054			*HcRHPortStatus[1]*	
31:21		0	Reserved	
20	R/W	0b	PRSC	Port Reset Status Change This bit is set at the end of the 10-ms port reset signal. Writing a 1 clears this bit. Write 0 has no effect. 0 = Port reset is not complete 1 = Port reset is complete
19	R/W	0b	OCIC	Port Over Current Indicator Change This bit is valid only if the per port overcurrent condition bit is set. This bit is set when the root hub changes the Port Over Current Indicator bit. Writing a 1 clears this bit. Write 0 has no effect. 0 = No change in Port Over Current Indicator 1 = Port Over Current Indicator has changed
18	R/W	0b	PSSC	Port Suspend Status Change This bit is set when the full resume sequence has been completed. The HCD writes 1 to clear this bit. Write 0 has no effect. This bit is also cleared when the Reset Status Change is set. 0 = Resume is not completed 1 = Resume completed
17	R/W	0b	PESC	Port Enable Status Change This bit is set when hardware events cause the PortEnableStatus bit to be cleared. Changes from Software writes do not set this bit. This bit is cleared by writing a 1. Write 0 has no effect. 0 = No change in Port Enable Status 1 = Change in Port Enable Status
16	R/W	0b	CSC	(R) Connect Status Change This bit is set whenever a connect or disconnect event occurs. 0 = No change in Current Connect Status 1 = Change in Current Connect Status (W) Clear Connect Status Change Writing a 1 clears this status bit. Write 0 has no effect.
15:10			Reserved	
9	R/W	NI	LSDA	(R) Low Speed Device Attached 0 = Full speed device is attached. 1 = Low speed device is attached. (W) Clear Port Power Writing a 1 clears the PPS bit. Write 0 has no effect.

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USB REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
8	R/W	0b	PPS	(R) Port Power Status 0 = Port power is off 1 = Port power is on. (W) Set Port Power Write 1 sets the bit. Write 0 has no effect.
7:5			Reserved	
4	R/W	0b	PRS	(R) Port Reset Status 0 = Port reset signal is not active. 1 = Port reset signal is active. This bit self clears after the PortResetStatusChange PRSC bit is set. (W) Set Port Reset Set the PRS bit by writing a 1 when CCS is 1. If CCS is a 0 when writing a 1, CSC bit will be set. Write 0 has no effect.
3	R/W	0b	POCI	(R) Port Over Current Indicator 0 = No overcurrent condition 1 = Overcurrent condition is detected. (W) Clear Suspend Status The HCD writes a 1 to resume and clear PSS. Write 0 has no effect.
2	R/W	0b	PSS	(R) Port Suspend Status. 0 = Port is not suspended. 1 = Port is suspended. This bit is cleared when Port Reset Status Change is set at the end of the port reset or when the HC is placed in the USB RESUME state. (W) Set Port Suspend When CCS is a 1, writing a 1 sets this bit. Write 0 has no effect. If CCS is 0 when writing a 1, CSC bit will be set instead.
1	R/W	0b	PES	(R) Port Enable Status 0 = Port is disabled. 1 = Port is enabled. (W) SetPortEnable. Writing a 1 sets this bit. CCS should be 1 to set this bit. If CCS is 0 while writing a 1 to this bit, only CSC bit will be set. This bit is also set if not already, at the completion of a port reset when Reset Status Change is set or port suspend when Suspend Status Change is set. Write 0 has no effect.
0	R/W	0b	CCS	(R) Current Connect Status 0 = No device connected. 1 = Device Connected. (W) Clear Port Enable. Reset PES bit by writing a 1. Write 0 has no effect.
Offset 0x04 8058			*HcRHPortStatus[2]*	
Note: All registers are identical to HcRHPortStatus[1]. See Address 0x04 8054 for register descriptions.				
Offset 0x04 807C			*Clock Control*	
31:12	R	0000h	Reserved	
11	W	0h	ClearStpClk	Writing 1 to this bit clears the USB Stop Clock bit. Writing a 0 has no effect.
10	W	0b	SetStpClk	Writing 1 to this bit sets the USB Stop Clock bit. Writing a 0 has no effect. Intended for software debug.
9	W	0b	ClearStrtClk	Write 1 to this bit, to clear the USB Start Clock bit. Writing a 0 has no effect

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USB REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
8	W	0b	SetStrtClk	Write 1 to this bit, to set the USB Start Clock bit. Writing a 0 has no effect. Intended for software debug.
7:2	R	00h	Reserved	
1	R	0b	StpClk	Indicates USB clocks may be stopped. This bit is reset by writing a 1 to bit 11.
0	R	0b	StrtClk	Indicates USB clocks should be started within 50 uS. This bit is cleared by writing a 1 to bit 9 of this register.
Offset 0x04 8FF4			*POWERDOWN*	
31	R/W	0	POWER_DOWN	Powerdown register for the module 0 = Normal operation of the peripheral. This is the reset value. 1 = Module is powered down and module clock can be removed. At powerdown, module responds to all reads with DEADABBA (except for reads of powerdown bit) and all writes with ERR ACK (except for writes to powerdown bit).
30:0		-	Unused	Ignore during writes and read as zeroes.
Offset 0x04 8FFC			*Module ID*	
31:16	R	0x0109	Module ID	Module ID assigned for USB
15:12	R	0	MajRev	Current major revision of this module
11:8	R	0	MinReV	Current minor revision of this module
7:0	R	0	ApertureSz	Aperture size of this module is 4kB.

IEEE 1394 Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.14)

IEEE 1394 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Global Control and Status Registers				
Offset 0x04 9000			*ID register (IDREG)*	
31:22	R/W	3FF	BUS_ID	The 10-bit bus number that is used with the Node ID in the source address for outgoing packets and used to accept or reject incoming packets.
21:16	R/W	3F	NODE_ID	Used in conjunction with BUS ID in the source address for outgoing packets. Used to accept or reject incoming packets. Automatically updated with the node ID assigned after the IEEE 1394 bus Tree-ID sequence.
15:8	R	02	PART_CODE	0x03 = VIPER 0x02 = PDI1394L41 0x01 = PDI1394L21
7:0	R	01	VERSION_CODE	Shows the revision of the IEEE 1394_AVLINK_CORE. 0x01 = current version of PDI1394L41

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IEEE 1394 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x04 9004			*General Link Control (LNKCTL)*	
31	R/W	0	IDVALID	When set to one, the IEEE 1394_AVLINK_CORE accepts the packets addressed to this node. Automatically set after self-ID is completed and node ID is updated.
30	R/W	1	RCVSELFID	When set to one, the self-ID packets generated by each PHY device on the bus during bus initialization are received and placed into the asynchronous request queue as a single packet. Also enables reception of PHY configuration packets in the asynchronous request queue.
29:27	R/W	0	BSYCTRL	These bits control what busy status the chip returns to incoming packets. 000 = Use protocol requested by received packet (either dual phase or single phase 001 = Send busyA when it is necessary to send a busy acknowledge (testing/diagnostics) 010 = Send busyB when it is necessary to send a busy acknowledge (testing/diagnostics) 011 = Use single phase retry protocol 100 = Use protocol requested in packet, always send a busy ack for all packets 101 = Busy A all incoming packets 110 = Busy B all incoming packets 111 = Use single phase retry protocol, always send a busy ack.
26	R/W	1	TxENABLE	Set to logic 1, the link layer transmitter will arbitrate and send bus packets.
25	R/W	1	RxENABLE	Set to logic 1, link layer transmitter will receive & respond to bus packets.
24:22		-	Unused	Bits read 0.
21	R/W	0	RSTTx	Reset the link layer transmitter.
20	R/W	0	RSTRx	Reset the link layer receiver.
19		-	Unused	Bits read 0.
18	R/W	0	RPL	Reset the PHY-LINK interface according to IEEE 1394.a requirements. This bit automatically resets to logic 0 after completion of the reset.
17:13		-	Unused	Bits read 0
12	R/W	0	STRICTISOCH	When set to logic 1, packets that are sent outside of specified isochronous cycles are rejected.
11	R/W	0	CYMASTER	When set and LNKCTL.ROOT = 1 and CYCTIM.CYCLENUMBER increments, the transmitter sends a cycle-start packet. The cycle master function will be disabled if a cycle timeout is detected (LNK-PHYINTACK. CYTMOUT = 1). To restart the cycle master function in such a case, first reset CYMASTER, then set it again.
10	R/W	0	CYSOURCE	1 = The CYCTM.CYCLENUMBER increments and CYCTM.CYCLE_ OFFSET resets for each positive transition of the cycle in port. 0 = The CYCTM.CYCLENUMBER increments when the CYCTM.CYCLE_ OFFSET rolls over.
9	R/W	0	CYTIMREN	Activates the CYCTM register when set.
8:7		-	Unused	
6	R/W	1	TxRDY	The transmitter is idle and ready.

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IEEE 1394 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
5	R	0	ROOT	When set, this node is the root on the IEEE 1394 bus. This bit is automatically updated after the self-ID phase.
4	R	0	BUSYFLAG	0 = Busy A will send once acknowledge is required. 1 = Busy B will send once acknowledge is required.
3:0	R	0	ATACK	At Acknowledge received. The last acknowledge received by the transmitter in response to a packet sent from the transmit-FIFO interface while ATF is selected (diagnostic purposes).
Offset 0x04 9008			*Link/PHY Interrupt Acknowledge (LNKPHYINTACK)*	
31:22		-	Unused	
21	R/W	0	CADONE	Interrupt from external source (ECA in case of L41)
20	R/W	0	TIMER	Interrupt when timer has counted to 0.
19		-	Unused	
18	R/W	0	CMDRST	Command Reset: a write request to RESET-START has been received.
17	R/W	0	FAIRGAP	The serial bus has been idle for a fair gap (called subaction gap in the IEEE 1394 Specification, Ref [3].
16	R/W	0	ARBGAP	The serial bus has been idle for an arbitration gap.
15	R/W	0	PHYINT	The PHY chip has signaled an interrupt through the PHY interface after a bus reset of PHY reset. Activates for any of the following reasons: (1) PHY has detected a loop on the bus. (2) Cable power has fallen below the minimum voltage. (3) PHY arbitration state machine has timed out, indicating a bus loop. (4) Bus cable has been disconnected. Recognition and notification of any of the above events by the PHY requires between 166 and 500 ms; so this bit is not instantaneously set.
14	R/W	0	PHYRRX	PHY register information received; register data has been transferred by the PHY into the Link.
13	R/W	0	PHYRST	PHY reset started. A PHY-layer reconfiguration has started. This interrupt clears the ID valid bit. It is called a Bus Reset in IEEE 1394 Specification, Ref [3]. The asynchronous queues will be flushed during a bus reset.
12:11		-	Unused	
10	R/W	0	ITBADFMT	Isochronous Transmitter is stuck. The transmitter has detected invalid data at the transmit FIFO interface when the ITF is selected. Reset the isochronous transmitter to clear.
9	R/W	0	ATBADFMT	Asynchronous Transmitter is stuck. The transmitter expected the start of a new asynchronous packet in the FIFO, but found other data (out of sync with user). Reset the asynchronous transmitter to clear.
8	R/W	0	SNTREJ	Busy acknowledge sent by receiver. The receiver was forced to send a busy acknowledge to a packet in this node because the receiver response/request FIFO overflowed.
7	R/W	0	HDRERR	Header error. The receiver detected a header CRC error on an incoming packet that may have been addressed to this node.
6	R/W	0	TCERR	Transaction Code Error. The transmitter detected an invalid transaction code in the data at the transmit FIFO interface.

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IEEE 1394 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
5	R/W	0	CYTMOUT	Cycle timed out. An isochronous cycle lasted more than 125 ms from cycle-start to fair gap. This disables the cycle master function.
4	R/W	0	CYSEC	Cycle second incremented. The CYCTM.CYCLE_SECONDS field has been incremented.
3	R/W	0	CYSTART	Cycle started. The transmitter has sent or the receiver has received a cycle start packet.
2	R/W	0	CYDONE	Cycle done. A fair gap has been detected on the bus after the transmission or reception of a cycle start packet. This indicates that the isochronous cycle is over.
1	R/W	0	CYPEND	Cycle pending is asserted when cycle timer offset is set to zero (rolled over or reset) and stays asserted until the isochronous cycle has ended.
0	R/W	0	CYLOST	Cycle lost. The cycle timer has rolled over twice without the reception of a cycle start packet. This only occurs when cycle master is not asserted.
Offset 0x04 900C			*Link/PHY Interrupt Enable (LNKPHYINTE)*	
Reference Offset 0x04 9008 Link/PHY Interrupt Acknowledge (LNKPHYINTACK) for more details.				
31:22		-	Unused	
21	R/W	0	EECA_INT	Enable interrupt from external source.
20	R/W	0	ETIMER	Enable interrupt when Timer has counted to 0.
19		-	Unused	
18	R/W	0	ECMDRST	Enable interrupt Command Reset Received.
17	R/W	0	EFAIRGAP	Enable interrupt to the serial bus that has been idle for a Fair Gap.
16	R/W	0	EARBGAP	Enable interrupt to the serial bus that has been idle for an Arbitration Gap.
15	R/W	0	EPHYINT	Enable interrupt to the PHY chip that has signaled an interrupt through the PHY interface after a bus reset of PHY reset.
14	R/W	0	EPHYRRX	Enable interrupt to PHY Register information Received.
13	R/W	0	EPHYRST	Enable interrupt to PHY Reset that has started.
12:11		-	Unused	
10	R/W	0	EITBADFMT	Enable interrupt when the Isochronous Transmitter is stuck.
9	R/W	0	EATBADFMT	Enable interrupt when the Asynchronous Transmitter is stuck.
8	R/W	0	ESNTREJ	Enable interrupt to Busy Acknowledge sent by receiver.
7	R/W	0	EHDRERR	Enable interrupt to Header Error.
6	R/W	0	ETCERR	Enable interrupt to Transaction Code Error.
5	R/W	0	ECYTMOUT	Enable interrupt to Cycle Timed Out.
4	R/W	0	ECYSEC	Enable interrupt to Cycle Second incremented.
3	R/W	0	ECYSTART	Enable interrupt to Cycle Started.
2	R/W	0	ECYDONE	Enable interrupt to Cycle Done.
1	R/W	0	ECYPEND	Enable interrupt to Cycle Pending.
0	R/W	0	ECYLOST	Enable interrupt to Cycle Lost.

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IEEE 1394 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x04 9010			*Cycle Timer Register (CYCTM)*	
31:25	R/W	0	CYCLE_SECONDS	Second counter
24:12	R/W	0	CYCLE_NUMBER	8 kHz bus cycle counter
11:0	R/W	0	CYCLE_OFFSET	24.576 MHz cycle counter
Offset 0x04 9014			*PHY Register Access (PHYACS)*	
31	R/W	0	RDPHY	When set, a read register request with accompanying address (RGPHYAD) is sent to the PHY. Bit is cleared after the request is sent.
30	R/W	0	WRPHY	When set, a write register request with accompanying address (RGPHYAD) and data (RGPHYDATA) is sent to the PHY. This bit is cleared after the request is sent.
29:28		-	Unused	
27:24	R/W	0	PHYRGAD	Address of the PHY register that is being accessed
23:16	R/W	0	PHYRGDATA	Data to be written to the PHY register PHYRGAD
15:12		-	Unused	
11:8	R	0	PHYRXAD	Address of register from which data (PHYRXDATA) was read
7:0	R	0	PHYRXDATA	Data as read from PHY register indicated in PHYRXAD
Offset 0x04 9018			*Global Interrupt Status and TX Control (GLOBCSR)*	
31:19		-	Unused	
20	R/W	0	SFTRST	1 = Generates a reset of the IEEE 1394 module, resetting all registers to their reset value. Automatically cleared after 2 cycles of CLK_1394. 0 = No effect
19		-	Unused	
18	R/W	0	ENOUTAV2	Controls the value of port enoutav2.
17	R/W	0	ENOUTAV1	Controls the value of port enoutav1.
16	R/W	1	DIRAV1	Controls the value of port dirav1.
15		-	Unused	
14	R/W	0	EITX1INT (see Note)	1 = Enables interrupt bit GLOBCSR.ITX1INT. 0 = Disables interrupt bit GLOBCSR.ITX1INT. Note: Bits EITX1INT and ITX1INT are only present when IEEE 1394_ AVLINK _ CORE has been ordered with two isochronous transmitters.
13:12		-	Unused	
11	R/W	0	EASYTX/RX	1 = Enables interrupt bit GLOBCSR.ASYTX/RX. 0 = Disables interrupt bit GLOBCSR.ASYTX/RX.
10	R/W	0	EITX0INT	1 = Enables interrupt bit GLOBCSR.ITX0INT. 0 = Disables interrupt bit GLOBCSR.ITX0INT.
9	R/W	0	EIRX0INT	1 = Enables interrupt bit GLOBCSR.IRX0INT. 0 = Disables interrupt bit GLOBCSR.IRX0INT.
8	R/W	0	ELNKPHYINT	1 = Enables interrupt bit GLOBCSR.LNKPHYINT. 0 = Disables interrupt bit GLOBCSR.LNKPHYINT.
7		-	Unused	

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IEEE 1394 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
6	R	0	ITX1INT (see Note)	1 = Signals that an interrupt is pending in the ITX1_INT register. 0 = No interrupt in ITX1_INT register is set.
5:4		-	Unused	
3	R	0	ASYTX/RX	1 = Signals that an interrupt is pending in the ASYINT register. 0 = No interrupt in ASYINT register is set.
2	R	0	ITX0INT	1 = Signals that an interrupt is pending in the ITX0_INT register. 0 = No interrupt in ITX0_INT register is set.
1	R	0	IRX0INT	1 = Signals that an interrupt is pending in the IRX0_INT register. 0 = No interrupt in IRX0_INT register is set.
0	R	0	LNKPHYINT	1 = Signals that an interrupt is pending in the LNKPHYINTACK register. 0 = No interrupt in LNKPHYINTACK register is set.
Offset 0x04 901C			*Timer (TIMER)*	
31	R/W	0	TMGOSTOP	1 = Start timer. This bit will be automatically reset to 0. 0 = No effect
30	R/W	0	TMCONT	1 = Continuously operate timer. 0 = Operate timer for one timing cycle, then stop.
29	R/W	0	TMBRE	Timer bus reset enable 1 = Start the timer at the beginning of a bus reset. 0 = Start the timer upon setting the TIMER.TMGOSTOP bit.
28:24		-	Unused	
23:0	R/W	0	PRELOAD	Timer preload value
Offset 0x04 9020			*Isochronous Transmit Packing Control and Status (ITXn_PKCTL)*	
31		-	Unused	
30	R/W	0	MLAN	mLAN mode bit 0 = Normal SYT timestamping operation is assumed. 1 = Sends SYT stamps with data payloads only. Additionally, the SYT value will automatically be incremented by two additional cycles.
29:28	R/W	0	TXAP_CLK	This field controls the frequency and mode of the isochronous transmitter application clock at the AV interface. 00 = An external application clock should be provided, itx_clkouten is de-asserted. 01 = Output frequency at irx_clkout = 24.576 MHz, itx_clkouten is asserted. 10 = Output frequency at irx_clkout = 12.288 MHz, itx_clkouten is asserted. 11 = Output frequency at irx_clkout = 6.144 MHz, itx_clkouten is asserted.
27:16	R/W	0	TRDEL	Transport delay. Value added to cycle timer to produce timestamps. Lower 4 bits add to upper 4 bits of cycle_offset, (Cycle Timer Register, CYCTM). Remainder adds to cycle_count field.
15:8	R/W	0	MAXBL	The (maximum) number of data blocks to be put in a payload.
7	R/W	0	ENXTMPSTP	Enable External Timestamp control. Allows an external timestamp (generated by the application) to be inserted in place of the link generated timestamp. Defaults to link generated timestamp.

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IEEE 1394 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
6:5	R/W	0	SYT_DELAY	Programmable delay of AV1FSYNC and AV2FSYNC. Each cycle is 1 bus cycle, 125 ms. Reset value is '00', a 3 cycle delay. 01 = 2 cycles 00 = 3 cycles 10 = 4 cycles 11 = Reserved
4	R/W	0	EN_ITX	Enables receipt of new application packets and generation of isochronous bus packets in every cycle. Also enables the Link Layer to arbitrate for the transmitter in each subsequent bus cycle. When this bit is disabled (0), the current packet will be transmitted and then the transmitter will shut down.
3:2	R/W	0	PM	Packing Mode. 00 = Variable sized bus packets, most generic mode 01 = Fixed size bus packets 10 = MPEG-2 packing mode 11 = No data, just CIP headers are transmitted.
1	R/W	0	EN_FS	Enables generation/insertion of SYT stamps (Timestamps) in CIP header.
0	R/W	0	RST_ITX	Setting this bit (RST_ITX) to '1' resets the transmitter. For synchronous reset of ITX to work properly, an itx_clkin must be present to ensure the reset bit is kept (programmed) HIGH for at least the duration of one itx_clkin period. Failure to do so may cause the application interface of this module to be improperly reset (or not reset at all). When reset is enabled, all bytes will be flushed from the FIFO and transmission will cease.
Offset 0x04 9024			*Common Isochronous Transmit Packet Header Quadlet 1(ITXn_HQ1)*	
31:24		-	Unused	
23:16	R/W	0	DBS	Size of data blocks in quadlets, from which AV payload is constructed (0 = 256 quadlets).
15:14	R/W	0	FN	Fraction Number. The encoding for the number of data blocks into which each source packet shall be divided. 00 = 1 data block 01 = 2 data blocks 10 = 4 data blocks 11 = 8 data blocks
13:11	R/W	0	QPC	Number of zero filled dummy quadlets to append to each source packet before it is divided into data blocks of the specified sized. The value QPC must be less than DBS and less than 2^{FN}.
10	R/W	0	SPH	Indicates that a 25-bit CYCTM based timestamp has to be inserted before each application packet.
9:0		-	Unused	
Offset 0x04 9028			*Common Isochronous Transmit Packet Header Quadlet 2 (ITXn_HQ2)*	
31:30		-	Unused	Bits read 0.
29:24	R/W	0	FMT	Value to be inserted in the FMT field in the AV header.
23:0	R/W	0	FDF/SYT	Value to be inserted in the FDF field. When the EN_FS bit in the Isochronous Packing Transmit Control and Status register (ITX_n_CTL) is set (=1), the lower 16 bits of this register are replaced by an SYT stamp if a rising edge on av<x>_fsync_in has been detected or all `1s' if no such edge was detected since the previous packet. The upper 8 bits are sent as they appear in the FDF register. When the EN_FS bit in the Transmit Control and Status register = 0, the full 24 bits can be set to any application specified value.

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IEEE 1394 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x04 902C			*Isochronous Transmitter Interrupt Acknowledge (ITXn_INTACK)*	
31:15		-	Unused	Bits read 0.
14	R/W	0	SYERR	An overflow occurred at the buffer that stores events at emi, odd/ even or itx_sysync. As a result, the content of the SY field in the isochronous packet header can not be properly synchronized with the isochronous payload. Recommended action is to reset the isochronous transmitter. The internal event buffer can store up to 3 events for the current FIFO content. An event is a state change for one of the mentioned inputs.
13	R/W	0	ODDEVN	A packet with an updated odd/even key has just been transmitted.
12	R/W	0	EMI	A packet with updated emi bits has just been transmitted.
11:10		-	Unused	Bits read 0.
9	R/W	0	ITX100LFT	Set when the number of empty quadlets in the itx FIFO <= 100. This interrupt will be disabled when the FIFO size <= 100 Quadlets.
8	R/W	0	ITX256LFT	Set when the number of empty quadlets in the itx FIFO <= 256. This interrupt will be disabled when the FIFO size <= 256 Quadlets.
7	R/W	0	ITX512LFT	Set when number of empty quadlets in the itx FIFO <= 512. This interrupt will be disabled when the size of the FIFO size <= 512 Quadlets.
6	R/W	0	TRMSYT	Interrupt on transmission of a SYT in CIP header quadlet 2
5	R/W	0	TRMBP	Interrupt on payload transmission/discard complete
4	R/W	0	DBCERR	Acknowledge interrupt on Data Block Count (DBC) synchronization loss.
3	R/W	0	INPERR	Acknowledge interrupt on input error (input data discarded).
2	R/W	0	DISCARD	Interrupt on lost cycle (payload discarded).
1	R/W	0	ITXFULL	Set when the itx FIFO is full, the number of empty quadlets = 0. This is a fatal error. It is recommended to reset and re-initialize the transmitter.
0	R/W	0	ITXEMPTY	Set when the number of quadlets in the itx FIFO containing valid data = 0
Offset 0x04 9030			*Isochronous Transmitter Interrupt Enable (ITXn_INTE)*	
Reference Offset 0x04 9008 Link/PHY Interrupt Acknowledge ITXn_INTACK for more details.				
31:15		-	Unused	
14	R/W	0	ESYERR	Enable interrupt when an overflow occurred at the buffer that stores events at emi, oddeven or itx_sysync.
13	R/W	0	EODDEVN	Enable Interrupt when a packet with an updated odd/even key has just been transmitted.
12	R/W	0	EEMI	Enable Interrupt when a packet with updated emi bits has just been transmitted.
11:10		-	Unused	
9	R/W	0	EITX100LFT	Enables Interrupt when number of empty quadlets in the itx FIFO <= 100.
8	R/W	0	EITX256LFT	Enables Interrupt when number of empty quadlets in the itx FIFO <= 256.
7	R/W	0	EITX512LFT	Enables Interrupt when number of empty quadlets in the itx FIFO <= 512.

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IEEE 1394 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
6	R/W	0	ETRMSYT	Enables Interrupt on transmission of a SYT in CIP header quadlet 2.
5	R/W	0	ETRMBP	Enables Interrupt on payload transmission/discard complete.
4	R/W	0	EDBCERR	Enables interrupt on Data Block Count (DBC) synchronization loss.
3	R/W	0	EINPERR	Enables interrupt on input error (input data discarded).
2	R/W	0	EDISCARD	Enables Interrupt on lost cycle (payload discarded).
1	R/W	0	EITXFULL	Enables Interrupt when itx FIFO is full, the number of empty quadlets = 0.
0	R/W	0	EITXEMPTY	Enables Interrupt when the number of quadlets in the itx FIFO containing valid data = 0
Offset 0x04 9034			*Isochronous Transmitter Control Register (ITXn_CTL)*	
31:21		-	Unused	
20	R/W	0	CPHREN	Enable encryption cipher 0 = Application packets will not be encrypted. 1 = Application packets will be encrypted by the embedded stream cipher which operates according to the 5C content protection protocol. The choice of encryption key is determined by the status of the ITX_n_CTL.EMI and the ITX_n_CTL.ODDEVEN fields.
19	R/W	0	EMIPE	EMI Pin Enable 0 = Use EMI bits from this register ITX_n_CTL.EMI. 1 = Use EMI value from ports itx_emi.
18:16		-	Unused	
15:14	R/W	0	TAG	Tag code to be inserted into the isochronous bus packet header 01 = IEC 61883 international standard data
13:8	R/W	0	CHANNEL	Isochronous channel number
7		-	Unused	
6		0	Reserved	This bit is reserved for future extension of the SPD field according to IEEE 1394.a definition.
5:4	R/W	0	SPD	Cable transmission speed (S100, S200, S400) =00, 100MB/s =01, 200MB/s =10, 400MB/s =11, reserved.
3:2	R/W	0	EMI[1..0]	The EMI field specifies the encryption mode for the data stream. Functionality of this field depends on the status of the ITX_n_CTL. CPHREN bit and the ITX_n_CTL.EMIPE bit. If ITX_n_CTL.CPHREN is logic 0 then this field is R/W and its value will be transmitted into SY[3:2] of the Isochronous packet header. If ITX_n_CTL.CPHREN is logic 1 and ITX_n_CTL.EMIPE is logic 1 then this field is read only and reads the current status of port itx_emi. If ITX_n_CTL.CPHREN is logic 1 and ITX_n_CTL.EMIPE is logic 0 then this field is R/ W.
1	R/W	0	ODDEVEN	Functionality of the ODDEVEN bit depends on the status of ITX_n_CTL.CPHREN. If ITX_n_CTL.CPHREN is logic 0 then the value of this bit will be transmitted into SY[1] of the Isochronous packet header. If ITX_n_CTL.CPHREN is logic 1 then toggling this bit will cause the cipher to swap its odd/even key. Upon reading this bit will reflect the odd/even status of the cipher, not the value that was last written into this bit.
0	R	0	SYSYNC	The SYSYNC bit reads the value to be inserted in bit 0 of the SY field of the isochronous packet header.

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IEEE 1394 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x04 9038			*Isochronous Transmitter Memory Status (ITXn_MEM)*	
31:7		-	Unused	
6	R	0	ITXM100LFT	Set when the number of empty quadlets in the itx FIFO<=100. Disabled when the FIFO size <= 128 Quadlets.
5	R	0	ITXM256LFT	Set when the number of empty quadlets in itx FIFO <= 256. Disabled when the FIFO size <= 256 Quadlets.
4	R	0	ITXM512LFT	Set when number of empty quadlets in itx FIFO <= 512. Disabled when the size of the FIFO size <= 512 Quadlets.
3	R	0	ITXMF	Set when the itx FIFO is full, the number of empty quadlets = 0.
2	R	0	ITXMAF	Set when the number of empty quadlets in the itx FIFO = 1.
1	R	1	ITXM5AV	Set when the number of empty quadlets in the itx FIFO >= 5.
0	R	1	ITXME	Set when the number of quadlets in the itx FIFO containing valid data = 0.
Offset 0x04 9040			*Isochronous Receiver UnPacking Control and Status (IRXn_PKCTL)*	
31:30		-	Unused	
29:28	R/W	0	RXAP_CLK	This field controls the frequency and mode of the isochronous receiver application clock at the AV interface. 00 = An external application clock should be provided, irx_clkouten is deasserted. 01=Output frequency at irx_clkout = 24.576 MHz, irx_clkouten is asserted. 10=Output frequency at irx_clkout = 12.288 MHz, irx_clkouten is asserted. 11=Output frequency at irx_clkout = 6.144 MHz, irx_clkouten is asserted
27:9		-	Unused	
8	R/W	0	SNDIMM	Send application packet Immediately. 1 = A received isochronous application packet containing a CRC error will be output immediately, without regard for the timestamp value. 0 = A received isochronous application packet will be output with respect to the timestamp value.
7	R/W	0	DIS_TSC	Disable Timestamp Checking. 1 = The timestamp accompanying a packet is output before the isochronous application packet for use by the application. This adds an extra quadlet to the received data stream; the application must be capable of handling these 4 extra bytes. 0 = A received isochronous application packet will be output with respect to the timestamp value.
6	R/W	1	RMVUAP	Remove unreliable packets 1 = Received unreliable application packets (CRC error, data length error), which will be removed from the memory. 0 = All received application packets will be delivered.
5	R	0	SPAV	Source packet available for delivery in buffer memory.
4	R/W	0	EN_IRX	Enable receiver operation. Value is only checked whenever a new bus packet arrives, so enable/disable while running is ‘graceful’, meaning any transfers in process will be completed before this bit is asserted.

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IEEE 1394 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
3:2	R/W	0	BPAD	Byte Padding. The value indicates the amount of byte to be removed from the last data quadlet of each source packet. This is in addition to quadlet padding.
1	R/W	0	EN_FS	Enable processing of SYT stamps (Timestamps) in CIP header.
0	R/W	1	RST_IRX	Setting this bit (RST_IRX) to '1' resets the receiver. In order for synchronous reset of IRX to work properly, irx_clkin must be present to ensure the reset bit is kept (programmed) HIGH for at least the duration of one irx_clkin period. Failure to do so may cause the application interface of this module to be improperly reset (or not reset at all). When a receiver reset is required, first disable the receiver IRX_n_PKCTL.EN_IRX, wait until RX FIFO is emptied, then perform the reset. This allows previously received packets to go to the application instead of being lost.
Offset 0x04 9044			*Common Isochronous Receiver Packet Header Quadlet 1(IRXn_HQ1)*	
31	R	0	E0	End of Header. Always set to 0 for first CIP header quadlet.
30	R	0	F0	Format. Always set to 0 for first CIP header quadlet.
29:24	R	0	SID	Source ID. Contains the node address of the sender of the isochronous data.
23:16	R	0	DBS	Size of data blocks in quadlets from which AV payload is constructed (0 = 256 quadlets)
15:14	R	0	FN	Fraction Number. The encoding for the number of data blocks into which each source packet has been divided: 00 = 1 data block 01 = 2 data blocks 10 = 4 data blocks 11 = 8 data blocks
13:11	R	0	QPC	Number of zero filled dummy quadlets appended to each source packet before it was divided into data blocks of the specified sized.
10	R	0	SPH	1 = A 25-bit CYCTM based timestamp is inserted before each application packet. 0 = A 16-bit CYCTM based timestamp is inserted.
9:0		-	Unused	Bits read 0.
Offset 0x04 9048			*Common Isochronous Receiver Packet Header Quadlet 2 (IRXn_HQ2)*	
31	R	0	E1	End of Header. Always set to 1 for the second CIP header quadlet.
30	R	0	F1	Format. Always set to 0 for the second CIP header quadlet.
29:24	R	0	FMT	Value to be inserted in the FMT field in the CIP header.
23:0	R	FFFF	FDF/SYT	When the IRX_n_PKCTL.EN_FS is set (=1), the lower 16 bits of this register are interpreted as SYT.
Offset 0x04 904C			*Isochronous Receiver Interrupt Acknowledge (IRXn_INTACK)*	
31:14		-	Unused	
13	R/W	0	ODDEVN	An odd/even key change has appeared in a bus packet that was received.
12	R/W	0	EMI	Set when the received EMI bit values have changed in a bus packet that was received.
11		-	Unused	

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IEEE 1394 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
10	R/W	0	IRX100LFT	Set when the number of empty quadlets in the irx FIFO <= 100. This interrupt will be disabled when the FIFO size <= 100 Quadlets.
9	R/W	0	IRX256LFT	Set when the number of empty quadlets in the irx FIFO <= 256. This interrupt will be disabled when the FIFO size <= 256 Quadlets.
8	R/W	0	IRX512LFT	Set when number of empty quadlets in the rtx FIFO <= 512. This interrupt will be disabled when the size of the FIFO size <= 512 Quadlets.
7	R/W	0	IRXFULL	Set when the irx FIFO is full and the number of empty quadlets = 0. This is a fatal error. Recommended action is to reset and re-initialize the receiver.
6	R/W	0	IRXEMPTY	Set when the number of quadlets in the irx FIFO containing valid data = 0.
5	R/W	0	FSYNC	A pulse was generated on the irx_fsync output (SYT expired).
4	R/W	0	SEQERR	A data block sequence error has occurred (DBC value incorrect).
3	R/W	0	CRCERR	An IEEE 1394 bus packet with a CRC error was received.
2	R/W	0	CIPTAGFLT	A Common Isochronous Packet with unknown header format was received (E,F bits).
1	R/W	0	RCVBP	A bus packet was received and processed correctly.
0	R/W	0	SQOV	Status queue overflow. This is a fatal error. Recommended action is to reset and reinitialize the receiver.
Offset 0x04 9050			*Isochronous Receiver Interrupt Enable (IRXn_INTE)*	
Reference Offset 0x04 9008 Link/PHY Interrupt Acknowledge IRXn_INTACK for more details.				
31:14		-	Unused	
13	R/W	0	EODDEVN	Enable interrupt when an odd/even key change has appeared in a bus packet that was received.
12	R/W	0	EEMI	Enable interrupt when the received EMI bit values have changed in a bus packet that was received.
11		-	Unused	
10	R/W	0	EIRX100LFT	Enable interrupt when number of empty quadlets in the irx FIFO <= 100.
9	R/W	0	EIRX256LFT	Enable interrupt when number of empty quadlets in the irx FIFO <= 256.
8	R/W	0	EIRX512LFT	Enable interrupt when number of empty quadlets in the rtx FIFO <= 512.
7	R/W	0	EIRXFULL	Enable interrupt when irx FIFO is full, the number of empty quadlets = 0.
6	R/W	0	EIRXEMPTY	Enable interrupt when the number of quadlets in the irx FIFO containing valid data = 0.
5	R/W	0	EFSYNC	Enable interrupt when a pulse was generated on the irx_fsync output (SYT expired).
4	R/W	0	ESEQERR	Enable interrupt when a data block sequence error has occurred (DBC value incorrect).
3	R/W	0	ECRCERR	Enable interrupt when a IEEE 1394 bus packet with a CRC error was received.

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IEEE 1394 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
2	R/W	0	ECIPTAGFLT	Enable interrupt when a Common Isochronous Packet with unknown header format was received (E,F bits).
1	R/W	0	ERCVBP	Enable interrupt when a bus packet was received and processed correctly.
0	R/W	0	ESQOV	Enable interrupt when status queue overflow occurs.
Offset 0x04 9054			*Isochronous Receiver Control Register (IRXn_CTL)*	
31:21		-	Unused	
20	R/W	0	DCPHREN	Enable encryption deciphering.
19:18		-	Unused	
17:16	R	0	SPD	Cable transmission speed (S100, S200, S400) 00 = 100MB/s 01 = 200MB/s 10 = 400MB/s 11 = reserved
15:14	R/W	0	TAG	Tag code as received in the isochronous bus packet header 01 = IEC 61883 international standard data.
13:8	R/W	0	CHANNEL	Isochronous channel number
7:4	R	0	ERR	Error code for the last receiver isochronous AV packet. 0001 = The node has successfully accepted the bus packet. 1101 = The node could not accept the bus packet because the payload failed the CRC check or because the length of the payload did not match the length that was specified in the isochronous packet header.
3:2	R	0	EMI[1..0]	EMI control bits
1	R	0	ODDEVEN	ODDEVEN control bit
0	R	0	SYSYNC	Bit 0 of the SY field of the isochronous packet header as received.
Offset 0x04 9058			*Isochronous Receiver Memory Status (IRXn_MEM)*	
31:7		-	Unused	
6	R	0	IRXM100LFT	Set when the number of empty quadlets in the itx FIFO <= 100. Disabled when the FIFO size <= 100 Quadlets.
5	R	0	IRXM256LFT	Set when the number of empty quadlets in itx FIFO <= 256. Disabled when the FIFO size <= 256 Quadlets.
4	R	0	IRXM512LFT	Set when number of empty quadlets in itx FIFO <= 512. Disabled when the size of the FIFO size <= 512 Quadlets.
3	R	0	IRXMF	Set when the itx FIFO is full, the number of empty quadlets = 0.
2	R	0	IRXMAF	Set when the number of empty quadlets in the itx FIFO = 1.
1	R	1	IRXM5AV	Set when the number of empty quadlets in the itx FIFO >= 5.
0	R	1	IRXME	Set when the number of quadlets in the itx FIFO containing valid data = 0.

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IEEE 1394 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Asynchronous Control and Status Interface Registers				
Offset 0x04 9080			*Asynchronous RX/TX Control (ASYCTL)*	
31	R/W	0	EN_LDTR	Controls how the transfer registers are being updated with new data from receive request queue and the receive response queue. In order to prevent speculative read actions by a CPU from destroying the FIFO contents, this bit should always be set to 1. 1 = The interrupt bit ASYINTACK.RRSPQQAV or ASYINTACK.RREQQQAV has to be cleared in order to load the latest data from the related queue into the transfer register. In this mode speculative read actions will not cause any harm to the contents of the FIFO. 0 = Reading a transfer register will cause the transfer register to immediately load the latest data from the related receive queue.
30:24		-	Unused	Bits read 0.
23	R/W	0	DIS_BCAST	Disable the reception of broadcast packets.
22	R/W	0	ARXRST	Asynchronous receiver reset. This bit will auto clear when the link layer state machine is idle.
21	R/W	1	ATXRST	Asynchronous transmitter reset. After every bus reset this bit is set to logic 1. This effectively disables the asynchronous transmitter. Re-enable the asynchronous transmitter by clearing this bit after each bus reset, especially if asynchronous transmission is used.
20	R/W	1	ARXALL	Receive and filter only RESPONSE packets. 1 = All responses are stored in the FIFO. 0 = Only solicited responses are stored in the FIFO.
19:16	R/W	0	MAXRC	Maximum number of asynchronous transmitter single phase retries.
15:13	R/W	0	TOS	Timeout Seconds, integer of 1 second
12:0	R/W	0320	TOF	Timeout Fractions, integer of 1/8000 second. Resets to 0x0320, which is 100 milliseconds.
Offset 0x04 9084			*Asynchronous RX/TX Memory Status (ASYMEM)*	
31:18		-	Unused	Bits read 0.
17	R	1	TRSPQIDLE	Set when the transfer register of the asynchronous transmitter response queue is empty.
16	R	1	TREQQIDLE	Set when the transfer register of the asynchronous transmitter request queue is empty.
15	R	0	RRSPQF	Set when the asynchronous receiver response FIFO is full, the number of empty quadlets = 0.
14	R	0	RRSPQAF	Set when the number of empty quadlets in the asynchronous receiver response FIFO=1.
13	R	1	RRSPQ5AV	Set when the number of empty quadlets in the asynchronous receiver response FIFO >= 5.
12	R	1	RRSPQE	Set when the number of quadlets in the asynchronous receiver response FIFO containing valid data = 0.
11	R	0	RREQQF	Set when the asynchronous receiver request FIFO is full, the number of empty quadlets = 0.
10	R	0	RREQQAF	Set when the number of empty quadlets in the asynchronous receiver request FIFO = 1.

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IEEE 1394 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
9	R	1	RREQQ5AV	Set when the number of empty quadlets in the asynchronous receiver request FIFO >= 5.
8	R	1	RREQQE	Set when the number of quadlets in the asynchronous receiver request FIFO containing valid data = 0.
7	R	0	TRSPQF	Set when the asynchronous transmitter response FIFO is full, the number of empty quadlets = 0.
6	R	0	TRSPQAF	Set when the number of empty quadlets in the asynchronous transmitter response FIFO= 1.
5	R	1	TRSPQ5AV	Set when the number of empty quadlets in the asynchronous transmitter response FIFO >= 5.
4	R	1	TRSPQE	Set when the number of quadlets in the asynchronous transmitter response FIFO containing valid data = 0.
3	R	0	TREQQF	Set when the asynchronous transmitter request FIFO is full, the number of empty quadlets = 0.
2	R	0	TREQQAF	Set when the number of empty quadlets in the asynchronous transmitter request FIFO = 1.
1	R	1	TREQQ5AV	Set when the number of empty quadlets in the asynchronous transmitter request FIFO >= 5.
0	R	1	TREQQE	Set when the number of quadlets in the asynchronous transmitter request FIFO containing valid data = 0.
Offset 0x04 9088			*Asynchronous Transmit Request Next (TX_RQ_NEXT)*	
31:0	W	0	TX_RQ_NEXT	First/Middle quadlet of packet for asynchronous transmitter request queue. Writing this register will clear the ASYINTACK.TRREQQWR flag until the quadlet has been written into its FIFO.
Offset 0x04 908C			*Asynchronous Transmit Request Last (TX_RQ_LAST)*	
31:0	W	0	TX_RQ_LAST	Last quadlet of packet for asynchronous transmitter request queue. Writing this register will clear the ASYINTACK.TRREQQWR flag until the quadlet has been written into its FIFO.
Offset 0x04 9090			*Asynchronous Transmit Response Next (TX_RP_NEXT)*	
31:0	W	0	TX_RP_NEXT	First/Middle quadlet of packet for asynchronous transmitter response queue. Writing this register will clear the ASYINTACK. TRRSPQWR flag until the quadlet has been written into its FIFO.
Offset 0x04 9094			*Asynchronous Transmit Response Last (TX_RP_LAST)*	
31:0	W	0	TX_RP_LAST	Last quadlet of packet for asynchronous transmitter response queue. Writing this register will clear the ASYINTACK. TRRSPQWR flag until the quadlet has been written into its FIFO.
Offset 0x04 9098			*Asynchronous Receive Request (RREQ)*	
31:0	R	0	RREQ	Quadlet of packet from asynchronous receiver request queue which resides in the transfer register. Reading this register will clear the ASYINTACK.RREQQQAV flag until the next received quadlet is available for reading.
Offset 0x04 909C			*Asynchronous Receive Response (RRSP)*	
31:0	R	0	RREQ	Quadlet of packet from asynchronous receiver response queue which resides in the transfer register. Reading this register will clear the ASYINTACK.RRSPQQAV flag until the next received quadlet is available for reading.

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IEEE 1394 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x04 90A0			*Asynchronous RX/TX Interrupt Acknowledge (ASYINTACK)*	
31:17		-	Unused	Bits read 0.
16	R/W	0	RRSPQFULL	Asynchronous receiver response queue has become full.
15	R/W	0	RREQQFULL	Asynchronous receiver request queue has become full.
14	R/W	0	SIDQAV	Current quadlet in the asynchronous receiver request queue is Self-ID data. This bit is set only after a bus reset, not after reception of PHY packets other than self-IDs. This interrupt automatically resets when the quadlet is read.
13	R/W	0	RRSPQLASTQ	Current quadlet in asynchronous receiver response queue is the last quadlet of a bus packet.
12	R/W	0	RREQQLASTQ	Current quadlet in asynchronous receiver request queue is the last quadlet of a bus packet.
11	R/W	1	RRSPQRDERR	Asynchronous receiver response queue read error (transfer error) or bus reset occurred. When set to logic 1, this queue is blocked for read access.
10	R/W	1	RREQQRDERR	Asynchronous receiver request queue read error (transfer error) or bus reset occurred. When set to logic 1, this queue is blocked for read access.
9	R/W	0	RRSPQQAV	Asynchronous receiver response queue quadlet is available.
8	R/W	0	RREQQQAV	Asynchronous receiver request queue quadlet is available.
7	R/W	0	TIMEOUT	Split transaction response timeout
6	R/W	0	RCVDRSP	Solicited response received (within timeout interval).
5	R/W	0	TRSPQFULL	Asynchronous transmitter response queue has become full.
4	R/W	0	TREQQFULL	Asynchronous transmitter request queue has become full.
3	R/W	0	TRSPQWRERR	Asynchronous transmitter response queue write error (transfer error)
2	R/W	0	TREQQWRERR	Asynchronous transmitter request queue write error (transfer error)
1	R/W	0	TRSPQWR	Asynchronous transmitter response queue written (transfer register emptied).
0	R/W	0	TREQQWR	Asynchronous transmitter request queue written (transfer register emptied).
Offset 0x04 90A4			*Asynchronous RX/TX Interrupt Enable (ASYINTE)*	
Reference Offset 0x04 9008 Link/PHY Interrupt Acknowledge ASYINTACK for more details.				
31:17		-	Unused	
16	R/W	0	ERRSPQFULL	Enable interrupt when the asynchronous receiver response queue has become full.
15	R/W	0	ERREQQFULL	Enable interrupt when the asynchronous receiver request queue has become full.
14	R/W	0	ESIDQAV	Enable interrupt when the current quadlet in the asynchronous receiver request queue is SelfID data.
13	R/W	0	ERRSPQLASTQ	Enable interrupt when the current quadlet in asynchronous receiver response queue is the last quadlet of a bus packet.
12	R/W	0	ERREQQLASTQ	Enable interrupt when the current quadlet in asynchronous receiver request queue is the last quadlet of a bus packet.

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IEEE 1394 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
11	R/W	1	ERRSPQRDERR	Enable interrupt when the asynchronous receiver response queue read error (transfer error) or bus reset occurred.
10	R/W	1	ERREQQRDERR	Enable interrupt when the asynchronous receiver request queue read error (transfer error) or bus reset occurred.
9	R/W	0	ERRSPQQAV	Enable interrupt when the asynchronous receiver response queue quadlet is available.
8	R/W	0	ERREQQQAV	Enable interrupt when the asynchronous receiver request queue quadlet is available.
7	R/W	0	ETIMEOUT	Enable interrupt when split transaction response timeout.
6	R/W	0	ERCVDRSP	Enable interrupt when the solicited response is received (within timeout interval).
5	R/W	0	ETRSPQFULL	Enable interrupt when the asynchronous transmitter response queue has become full.
4	R/W	0	ETREQQFULL	Enable interrupt when the asynchronous transmitter request queue has become full.
3	R/W	0	ETRSPQWRERR	Enable interrupt when the asynchronous transmitter response queue write error (transfer error).
2	R/W	0	ETREQQWRERR	Asynchronous transmitter request queue write error (transfer error).
1	R/W	0	ETRSPQWR	Enable interrupt when the asynchronous transmitter response queue written (transfer register emptied).
0	R/W	0	ETREQQWR	Enable interrupt when the asynchronous transmitter request queue written (transfer register emptied).
Registers for FIFO Size Programming				
Offset 0x04 9100			*Asynchronous Receive Response Fifo Size (RRSPSIZE)*	
31:14		-	Unused	
13:8	R/W	0	base_fifo	Base address of the FIFO
7:6		-	Unused	
5:0	R/W	03	end_fifo	End address of the FIFO
Offset 0x04 9104			*Asynchronous Receive Request Fifo Size (RREQSIZE)*	
31:14		-	Unused	
13:8	R/W	04	base_fifo	Base address of the FIFO
7:6		-	Unused	
5:0	R/W	07	end_fifo	End address of the FIFO
Offset 0x04 9110			*Asynchronous Transmit Response Fifo Size (TRSPSIZE)*	
31:14		-	Unused	
13:8	R/W	08	base_fifo	Base address of the FIFO
7:6		-	Unused	
5:0	R/W	0B	end_fifo	End address of the FIFO
Offset 0x04 9114			*Asynchronous Transmit Request Fifo Size (TREQSIZE)*	
31:14		-	Unused	
13:8	R/W	0C	base_fifo	Base address of the FIFO
7:6		-	Unused	

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IEEE 1394 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
5:0	R/W	0F	end_fifo	End address of the FIFO
Offset 0x04 9120			*Isochronous Receiver Fifo Size (IRX0_SIZE)*	
31:14		-	Unused	Bits read 0.
13:8	R/W	10	base_fifo	Base address of the FIFO
7:6		-	Unused	Bits read 0.
5:0	R/W	1F	end_fifo	End address of the FIFO
Offset 0x04 9130			*Isochronous Transmitter Fifo Size (ITX0_SIZE)*	
31:14		-	Unused	Bits read 0.
13:8	R/W	20	base_fifo	Base address of the FIFO
7:6		-	Unused	Bits read 0.
5:0	R/W	2F	end_fifo	End address of the FIFO
Offset 0x04 9134			*Isochronous Transmitter Fifo Size (ITX1_SIZE)*	
31:14		-	Unused	Bits read 0.
13:8	R/W	20	base_fifo	Base address of the FIFO
7:6		-	Unused	Bits read 0.
5:0	R/W	2F	end_fifo	End address of the FIFO
Offset 0x04 9138—91FC			*Reserved*	

IEEE 1394 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Copy No More Even/Odd Key Registers				
Offset 0x04 9200			*ITX0_CNMKE1*	
31:24		-	Unused	Bits read 0.
23:0	R/W	NI	Key 1	Holds bits [56:32] of the even No More Copies encryption key.
Offset 0x04 9204			*ITX0_CNMKE2*	
31:0	R/W	NI	Key 2	Holds bits [31:0] of the even No More Copies encryption key.
Offset 0x04 9208			*ITX0_COGKE1*	
31:24		-	Unused	Bits read 0.
23:0	R/W	NI	Key 1	Holds bits [56:32] of the even Copy One Generation encryption key.
Offset 0x04 920C			*ITX0_COGKE2*	
31:0	R/W	NI	Key 2	Holds bits [31:0] of the even Copy One Generation encryption key.
Offset 0x04 9210			*ITX0_CNKE1*	
31:24		-	Unused	Bits read 0.
23:0	R/W	NI	Key 1	Holds bits [56:32] of the even Copy Never encryption key.
Offset 0x04 9214			*ITX0_CNKE2*	
31:0	R/W	NI	Key 2	Holds bits [31:0] of the even Copy Never encryption key.

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IEEE 1394 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x04 9218			*ITX0_CNMKO1*	
31:24		-	Unused	Bits read 0.
23:0	R/W	NI	Key 1	Holds bits [56:32] of the odd No More Copies encryption key.
Offset 0x04 921C			*ITX0_CNMKO2*	
31:0	R/W	NI	Key 2	Holds bits [31:0] of the odd No More Copies encryption key.
Offset 0x04 9220			*ITX0_COGKO1*	
31:24		-	Unused	Bits read 0.
23:0	R/W	NI	Key 1	Holds bits [56:32] of the odd Copy One Generation encryption key.
Offset 0x04 9224			*ITX0_COGKO2*	
31:0	R/W	NI	Key 2	Holds bits [31:0] of the odd Copy One Generation encryption key.
Offset 0x04 9228			*ITX0_CNKO1*	
31:24		-	Unused	Bits read 0.
23:0	R/W	NI	Key 1	Holds bits [56:32] of the odd Copy Never encryption key.
Offset 0x04 922C			*ITX0_CNKO2*	
31:0	R/W	NI	Key 2	Holds bits [31:0] of the odd Copy Never encryption key.
Offset 0x04 9240			*ITX1_CNMKE1*	
31:24		-	Unused	Bits read 0.
23:0	R/W	NI	Key 1	Holds bits [56:32] of the even No More Copies encryption key.
Offset 0x04 9244			*ITX1_CNMKE2*	
31:0	R/W	NI	Key 2	Holds bits [31:0] of the even No More Copies encryption key.
Offset 0x04 9248			*ITX1_COGKE1*	
31:24		-	Unused	Bits read 0.
23:0	R/W	NI	Key 1	Holds bits [56:32] of the even Copy One Generation encryption key.
Offset 0x04 924C			*ITX1_COGKE2*	
31:0	R/W	NI	Key 2	Holds bits [31:0] of the even Copy One Generation encryption key.
Offset 0x04 9250			*ITX1_CNKE1*	
31:24		-	Unused	Bits read 0.
23:0	R/W	NI	Key 1	Holds bits [56:32] of the even Copy Never encryption key.
Offset 0x04 9254			*ITX1_CNKE2*	
31:0	R/W	NI	Key 2	Holds bits [31:0] of the even Copy Never encryption key.
Offset 0x04 9258			*ITX1_CNMKO1*	
31:24		-	Unused	Bits read 0.
23:0	R/W	0	Key 1	Holds bits [56:32] of the odd No More Copies encryption key.
Offset 0x04 925C			*ITX1_CNMKO2*	
31:0	R/W	NI	Key 2	Holds bits [31:0] of the odd No More Copies encryption key.
Offset 0x04 9260			*ITX1_COGKO1*	
31:24		-	Unused	Bits read 0.
23:0	R/W	NI	Key 1	Holds bits [56:32] of the odd Copy One Generation encryption key.

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IEEE 1394 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x04 9264			*ITX1_COGKO2*	
31:0	R/W	NI	Key 2	Holds bits [31:0] of the odd Copy One Generation encryption key.
Offset 0x04 9268			*ITX1_CNKO1*	
31:24		-	Unused	Bits read 0.
23:0	R/W	NI	Key 1	Holds bits [56:32] of the odd Copy Never encryption key.
Offset 0x04 926C			*ITX1_CNKO2*	
31:0	R/W	NI	Key 2	Holds bits [31:0] of the odd Copy Never encryption key.
Offset 0x04 9300			*IRX0_CNMKE1*	
31:24		-	Unused	Bits read 0.
23:0	R/W	NI	Key 1	Holds bits [56:32] of the even No More Copies encryption key.
Offset 0x04 9304			*IRX0_CNMKE2*	
31:0	R/W	NI	Key 2	Holds bits [31:0] of the even No More Copies encryption key.
Offset 0x04 9308			*IRX0_COGKE1*	
31:24		-	Unused	Bits read 0.
23:0	R/W	NI	Key 1	Holds bits [56:32] of the even Copy One Generation encryption key.
Offset 0x04 930C			*IRX0_COGKE2*	
31:0	R/W	NI	Key 2	Holds bits [31:0] of the even Copy One Generation encryption key.
Offset 0x04 9310			*IRX0_CNKE1*	
31:24		-	Unused	Bits read 0.
23:0	R/W	NI	Key 1	Holds bits [56:32] of the even Copy Never encryption key.
Offset 0x04 9314			*IRX0_CNKE2*	
31:0	R/W	NI	Key 2	Holds bits [31:0] of the even Copy Never encryption key.
Offset 0x04 9318			*IRX0_CNMKO1*	
31:24		-	Unused	Bits read 0.
23:0	R/W	NI	Key 1	Holds bits [56:32] of the odd No More Copies encryption key.
Offset 0x04 931C			*IRX0_CNMKO2*	
31:0	R/W	NI	Key 2	Holds bits [31:0] of the odd No More Copies encryption key.
Offset 0x04 9320			*IRX0_COGKO1*	
31:24		-	Unused	Bits read 0.
23:0	R/W	NI	Key 1	Holds bits [56:32] of the odd Copy One Generation encryption key.
Offset 0x04 9324			*IRX0_COGKO2*	
31:0	R/W	NI	Key 2	Holds bits [31:0] of the odd Copy One Generation encryption key.
Offset 0x04 9328			*IRX0_CNKO1*	
31:24		-	Unused	Bits read 0.
23:0	R/W	NI	Key 1	Holds bits [56:32] of the odd Copy Never encryption key.
Offset 0x04 932C			*IRX0_CNKO2*	
31:0	R/W	NI	Key 2	Holds bits [31:0] of the odd Copy Never encryption key.

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IEEE 1394 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x04 9FF4			*POWER_DOWN*	
31	R/W	0	PowerDown	0 = Normal operation of the peripheral. 1 = Module is powered down and the module clock can be removed. Module responds to all reads with DEADABBA (except for read of POWER_DOWN) and all writes with ERR ack (except for writes to POWER_DOWN)
30:0		-	Unused	Bits read 0.
Module ID Register				
Offset 0x04 9FFC			*MODULE_ID*	
31:16	R	0x0101	Module ID	Module ID
15:12	R	1	MajRev	Major revision indicates any revisions that break software compatibility of the IEEE 1394 module.
11:8	R	0	MinRev	Minor revision indicates any revisions that maintain software compatibility of the IEEE 1394 module.
7:0	R	0	ApertureSize	Size = 4 kB* (ApertureSize + 1)

UART 1 Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.11)

UART 1 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
UART 1 Registers (Offset 0x04 A000), UART 2 Registers (Offset 0x04 B000) and UART 3 Registers (Offset 0x04 C000) The UART 1, 2 and 3 registers are identical except for their offsets. A triplicate set has been created to facilitate programming. The tables for UART 2 (0x04 B000) and UART 3 (0x04 C000) registers follow the UART 1 register tables.				
Offset 0x04 A000			*Data Control Register*	
31		-	Unused	
30	R/W	0	TXBREAK	Transmission Break initiation. This is the Break Control bit. It causes a break condition to be transmitted to the receiving UART. The break is disabled by setting this bit to a logic 0. The Break Control bit acts only on TXD and has no effect on the transmitter logic. Note: This feature enables the CPU to alert a terminal in a computer communications system. 1. Set break when transmitter is empty. 2. Load all 0s into transmitter. 3. Wait for the transmitter to be idle, and clear break when normal transmission has to be restored.
29		-	Unused	
28	R/W	0	EVENPARITY	Even Parity Select. Setting this bit selects even parity instead of odd parity, if the ENPARITY bit is set.
27	R/W	0	ENPARITY	Parity Enable Bit. Setting this bit will cause parity to be generated and received.
26	R/W	0	TWOSTOP	Number of stop bits. Setting this bit will cause the transmitter to transmit two stop bits instead of one stop bit.
25		-	Unused	

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UART 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
24	R/W	0	BIT_8	Word select bit 0 = 7 bits per character mode 1 = 8 bits per character mode
23:22	R/W	0	FIFO_THRES	Set the trigger level for RCVR FIFO Interrupt (RX_INT) 23:22 Trigger Level (in decimal value) 00 01 01 04 10 08 11 14
21:19		-	Unused	
18	W	0	TX_FIFO_RST	Writing a “1” to this bit clears all the transmitter FIFO counters (pointer and status) to zero. This bit is self-clearing.
17	W	0	RX_FIFO_RST	Writing a “1” to this bit clears all the receiver FIFO counters (pointer and status) to zero. This bit is self-clearing.
16	W	0	RX_FIFO_PT_ADV	Writing a “1” to this bit advances the RX FIFO read pointer. This bit is self-clearing.
15:0		-	Unused	
Offset 0x04 A004			*Modem Control and Status Register*	
31:24	R/W	0	SCR	Scratch register - for software use
23	R	0	DCD	Data Carrier Detect is the complement to the DCDN input pin.
22:21		-	Unused	
20	R	0	CTS	This bit is the complement to the CTSN input pin. Software has to monitor this bit to know when the data carrier (e.g. modem, etc.) has room to receive data. If the Loop bit (reg 0x004 bit [4]) is set, CTS is equivalent to RTS. IF CTSENABLE (reg 0x00C bit [5]) is set, the automatic hardware flow control is enabled and the transmitter stops automatically if CTS is inactive.
19:5		-	Unused	
4	R/W	0	LOOP	Loopback mechanism. Setting this bit will cause the transmitted data to internally loopback to the receive data and the request_to_send signal to the clear_to send signal. The external UA_TXD output pin is held high and the external UA_DTRN output pin is held low when this bit is set
3:2		-	Unused	
1	R/W	0	RTS	Request to Send. This bit controls the Request To Send (RTSN) output. When this bit is set to a logic 1, the RTSN output is forced to a logic 0 (UART has characters to transmit). When this bit is reset to a logic 0, the RTSN output is forced to a logic 1. (There are no characters to transmit.) Note: RTSENABLE (reg 0x00C bit [4]) set the hardware flow control of the RTSN output. In this case, writing to this bit will have no effect on the RTSN output.
0	R/W	0	DTR	Data Terminal Ready. This bit is the complement to the DTRN output pin. Software set and reset. No hardware support required.
Offset 0x04 A008			*Baud Rate Register*	
31:16		-	Unused	

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UART 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
15:0	R/W	0000	BAUDRATE	The standard baud rates are determined as follows: Baud Rate = UART_CLOCK (default = 3. 6923 MHz) / ((BAUDRATE(15:0) + 1) * 16). A change of this value during operation will become effective after one baud cycle (1/baud rate) with the current baud rate. [15:0] Baud rate Percent Error 0 230400 0.002 1 115200 0.002 3 57600 0.002 5 38400 0.002 11 19200 0.002 23 9600 0.002 47 4800 0.002 95 2400 0.002 191 1200 0.002 383 600 0.002 767 300 0.002 1535 150 0.002 1715 134.5 0 2095 110 0.001 3071 75 0.002 4609 50 0.001
Offset 0x04 A00C			*Configuration Register*	
31:16	R/W	0004	RXTOCNTR	RX Timeout Control bits RX TimeOut = (RXTOCNTR[15:0]) * Character transmission time
15		-	Unused	
14	R/W	0	TXDMALOOPEN	The DMA channel TX controller supports two modes depending on the state of this bit. When DMALOOPEN is “0”, the DMA channel TX controller will stop executing when it reaches the end of the DMA buffer. When DMALOOPEN is “1”, the DMA controller will loopback to the start of the DMA buffer when the end of the DMA buffer is reached and will continue operating.
13	R/W	0	TXDMAPAUSE	Setting this bit will pause the current DMA transfer but it still allows the ongoing byte transfer(s) to be finished.The TX/RX register (0x028) and TX DMA Counter register (0x018) are accessible by software. When the bit is cleared the DMA operation will resume from where it stopped.
12	R/W	0	TXDMAEN	Enables the DMA channel TX transmit function. It should not be set until the START and LENGTH registers are set, module is enabled, and empty flag is set. When DMA operation is finished, software has to clear this bit and enable it for another DMA read operation. The DMA operation will abort if this bit is disabled prematurely. All the read bytes that were received (equal the TX DMA Length minus the content of the TX DMA Counter register) will be transmitted.
11		-	Unused	
10	R/W	0	RXDMALOOPEN	The DMA channel RX controller supports two modes depending on the state of this bit. When DMALOOPEN is “0”, the DMA channel RX controller will stop executing when it reaches the end of the DMA buffer. When DMALOOPEN is “1”’, the DMA controller will loopback to the start of the DMA buffer when the end of the DMA buffer is reached and will continue operating.

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UART 1 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
9	R/W	0	RXDMAPAUSE	Setting this bit will pause the current DMA transfer but it still allows the ongoing byte transfer to be finished. The RX/TX register (0x028) and RX DMA Counter register (0x024) are accessible by software. When the bit is cleared the DMA operation will resume from where it stopped.
8	R/W	0	RXDMAEN	Enables the DMA channel RX receive function. It should not be set until the START and LENGTH registers are set, module is enabled. and empty flag is set. When the DMA operation is finished, software has to clear this bit and enable it for another DMA write operation. The DMA operation will abort if this bit is disabled prematurely. All the written bytes that were sent (equal the RX DMA LENGTH minus the content of the RX DMA Counter register) will be flushed to the memory.
7:6		-	Unused	
5	R/W	0	CTSENABLE	Automatic CTSN processing (hardware flow control) is enabled when this bit is ‘1.’ When the computer (terminal) wishes to send data it activates the Request to Send line (set register 0x0004 bit [1], RTS, and disables RTSENABLE, register 0x000c bit [4]). If the carrier has room for data, the carrier will reply by activating the Clear to Send line and the computer will begin sending data. When this bit is set, the CTSN pin is evaluated automatically and the UART starts the transfer.
4	R/W	0	RTSENABLE	This bit enables the automatic generation of the RTSN signal. RTSN is active when the UART can receive characters (e.g., FIFO is not full). This option should be used if the UART is acting as a data carrier and is asked by the terminal if it is able to receive data.
3	R/W	0	RXBREAKHALT	Setting this bit will cause the receiver to halt (no more data is allowed to get into the receiver FIFO) after receiving a break, until the receiver FIFO is emptied and the UARTRXD signal goes to the marking state (’1’). Otherwise, the receiver will hold until the UARTRXD signal goes to the marking state without regard for the state of the Receiver FIFO.
2	R/W	0	DTINVERT	Setting this bit will cause the UARTTXD and UARTRXD signals to be inverted.
1	R/W	0	TXDDIS	Setting this bit will cause the UARTTXD signal to go low.
0		-	Unused	
Offset 0x04 A010			*TX DMA TX Start Address Register*	
31:0	R/W	0000	TXSTART	These bits define the start address for the DMA buffer for DMA transfers from the receiver FIFO. The value has to be the physical address.
Offset 0x04 A014			*TX DMA Length Register*	
31:12		-	Unused	
11:0	R/W	0000	TXLENGTH - 1	Length of DMA buffer in bytes (number of bytes to be transferred) minus 1. The last address in the DMA buffer is given by TXSTART + (TXLENGTH - 1).
Offset 0x04 A018			*TX DMA Counter Register*	
31:13		-	Unused	
12:0	R	0000	TXCOUNTER	TXDMA countdown counter value in bytes decrements from TXLENGTH to zero. This register will be reloaded with new “TXLENGTH” value when a new DMA operation gets started.
Offset 0x04 A01C			*RX DMA Start Address Register*	

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UART 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
31:0	R/W	0000	RXSTART	These bits define the start address for the transmitter DMA buffer. The value has to be the physical address.
Offset 0x04 A020			*RX DMA Length Register*	
31:16		-	Unused	
15:0	R/W	0000	RXLENGTH - 1	Length of DMA buffer in bytes (number of bytes to be transferred) minus 1. The last address in the DMA buffer is given by RXSTART + (RXLENGTH - 1).
Offset 0x04 A024			*RX DMA Counter Register*	
31:17		-	Unused	
16:0	R	0000	RXCOUNTER	RXDMA countdown counter value in bytes decrements from RXLENGTH to zero. This register will be reloaded with new “RXLENGTH” value when a new DMA operation gets started.
Offset 0x04 A028			*RBR/THR/FIFOS Receive/Transmit and FIFO Status Register*	
31:21		-	Unused	
20:16	R	0	TXFIFO_STA	TXFIFO Status: 5’h10 indicates 16 bytes remaining in the TX FIFO. 5’h0 indicates the TX FIFO is empty. These bits are reset by writing a “1” to bit [18] of register 0x000.
15:13		-	Unused	
12:8	R	0	RXFIFO_STA	RXFIFO Status: 5’h10 indicates 16 bytes remaining in the RX FIFO (5’h0 indicates the RX FIFO is empty). These bits are reset by writing a “1” to bit [17] of register 0x000.
7:0	R	00	RBR	Receiver Buffer register. Reading this register will not clear the RX_INT interrupt. Software should write a “1” to bit[16] of register 0x000 (RX_FIFO_PT_ADV bit) in order to advance the RX FIFO read pointer for the next read.
7:0	W		THR	Transmit Holding register
Offset 0x04 AFE0			*Interrupt Status Register*	
31:14		-	Unused	
13	R	0	TXDMAF_INT	Issues an interrupt when the TX DMA controller reaches the end of specified buffer (TXCOUNTER=0).
12	R	0	TXDMAH_INT	Issues an interrupt when the TX DMA controller reaches the halfway point in specified buffer (TXCOUNTER = TXLENGTH/2 if TXLENGTH is even and TXCOUNTER = TXLENGTH/2 - 1 if TXLENGTH is odd).
11	R	0	RXDMAF_INT	Issues an interrupt when the RX DMA controller reaches the end of specified buffer (RXCOUNTER=0).
10	R	0	RXDMAH_INT	Issues an interrupt when RX DMA controller reaches the halfway point in the specified buffer (RXCOUNTER = RXLENGTH/2 if RXLENGTH is even and RXCOUNTER = RXLENGTH/2 - 1 if RXLENGTH is odd).
9	R	0	DDCD_INT	This bit is high if the value of the DCDN input pin has changed.
8	R	0	DCTS_INT	This bit is high if the value of the CTSN input pin has changed.
7	R	0	TX_INT	Issues an interrupt when transmitter holding FIFO becomes empty.
6	R	0	EMPTY_INT	Issues an interrupt when the transmitter shift register becomes empty and the transmitter holding FIFO is also empty.

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UART 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
5	R	0	RCVTO_INT	Issues an interrupt when the receiver times out (timeout is equal to (RXTOCNTR[15:0]) *character transmission times) and no data is written to or read from the RX FIFO, and the RX FIFO is not empty.
4	R	0	RX_INT	Issues an interrupt when the threshold level is reached (the threshold level is set by writing to bits [23:22] of register 0x000).
3	R	0	RXOVRN_INT	Receiver Overflow issues an interrupt when the receiver holding FIFO is full and a new receive data is coming.
2	R	0	FRERR_INT	Frame Error Issues an interrupt when receiver does not detect stop bit following the character and received character is not 0x00.
1	R	0	BREAK_INT	Issues an interrupt when receiver detects a BREAK condition i.e., received character is 0x00 and no stop bit.
0	R	0	PARITY_INT	Issues an interrupt when receiver detects parity bit error.
Offset 0x04 AFE4			*Interrupt Enable Register*	
31:14		-	Unused	
13:0	R/W	0000	INTR_EN	A logic “1” written to a specific bit location will enable the corresponding interrupt in the Interrupt Status register.
Offset 0x04 AFE8			*Interrupt Clear Register*	
31:14		-	Unused	
13:0	W	0000	INTR_CLR	A logic “1” written to a specific bit location will clear the corresponding interrupt in the Interrupt Status register.This bit is self-clearing.
Offset 0x04 AFEC			*Interrupt Set Register*	
31:14		-	Unused	
13:0	W	0000	INTR_SET	A logic “1” written to a specific bit location will set the corresponding interrupt in the Interrupt Status register.
Offset 0x04 AFF4			*Powerdown Register*	
31	R/W	0	PD	UART Powerdown indicator 1 = Powerdown 0 = Power up When this bit equals 1, no other registers are accessible.
30:0		-	Unused	
Offset 0x04 AFFC			*Module ID Register*	
31:16	R	0x0107	MOD_ID	UART Module ID Number
15:12	R	0	REV_MAJOR	Major revision
11:8	R	0	REV_MINOR	Minor revision
7:0	R	0	APP_SIZE	Aperture size is 0 = 4 kB.

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UART 2 Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.11)

UART 2 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
UART 1 Registers (Offset 0x04 A000), UART 2 Registers (Offset 0x04 B000), and UART 3 Registers (Offset 0x04 C000) The UART 1, 2 and 3 registers are identical except for their offsets. A triplicate set has been created to facilitate programming. The tables for UART 1 (0x04 A000) and UART 3 (0x04 C000) registers precede and follow the UART 2 register tables respectively.				
Offset 0x04 B000			*Data Control Register*	
Offset 0x04 B004			*Modem Control and Status Register*	
Offset 0x04 B008			*Baud Rate Register*	
Offset 0x04 B00C			*Configuration Register*	
Offset 0x04 B010			*TX DMA TX Start Address Register*	
Offset 0x04 B014			*TX DMA Length Register*	
Offset 0x04 B018			*TX DMA Counter Register*	
Offset 0x04 B01C			*RX DMA Start Address Register*	
Offset 0x04 B020			*RX DMA Length Register*	
Offset 0x04 B024			*RX DMA Counter Register*	
Offset 0x04 B028			*RBR/THR/FIFOS Receive/Transmit and FIFO Status Register*	
Offset 0x04 BFE0			*Interrupt Status Register*	
Offset 0x04 BFE4			*Interrupt Enable Register*	
Offset 0x04 BFE8			*Interrupt Clear Register*	
Offset 0x04 BFEC			*Interrupt Set Register*	
Offset 0x04 BFF4			*Powerdown Register*	
Offset 0x04 BFFC			*Module ID Register*	

UART 3 Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.11)

UART 3 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
UART 1 Registers (Offset 0x04 A000), UART 2 Registers (Offset 0x04 B000), and UART 3 Registers (Offset 0x04 C000) The UART 1, 2 and 3 registers are identical except for their offsets. A triplicate set has been created to facilitate programming. The tables for UART 1 (0x04 A000) and UART 2 (0x04 B000) registers precede the UART 3 register table.				
Offset 0x04 C000			*Data Control Register*	
Offset 0x04 C004			*Modem Control and Status Register*	
Offset 0x04 C008			*Baud Rate Register*	
Offset 0x04 C00C			*Configuration Register*	
Offset 0x04 C010			*TX DMA TX Start Address Register*	

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UART 3 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x04 C014			*TX DMA Length Register*	
Offset 0x04 C018			*TX DMA Counter Register*	
Offset 0x04 C01C			*RX DMA Start Address Register*	
Offset 0x04 C020			*RX DMA Length Register*	
Offset 0x04 C024			*RX DMA Counter Register*	
Offset 0x04 C028			*RBR/THR/FIFOS Receive/Transmit and FIFO Status Register*	
Offset 0x04 CFE0			*Interrupt Status Register*	
Offset 0x04 CFE4			*Interrupt Enable Register*	
Offset 0x04 CFE8			*Interrupt Clear Register*	
Offset 0x04 CFEC			*Interrupt Set Register*	
Offset 0x04 CFF4			*Powerdown Register*	
Offset 0x04 CFFC			*Module ID Register*	

Global 2 Registers

GLOBAL 2 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Devices Controlled or Accessible by TM32 Registers *(PNX8526 User Manual, Ref. UM10104_1, Chap.2)*				
Offset 0x04 D000			*TM OWNED M-PI*	
31:20		-	Unused	Ignore during writes and read as zeroes.
19	R/W	0x1	TM_OWNED_GLBREG_1	0 = TriMedia does not have access to Global 1 MMIO aperture. 1 = TriMedia has access to Global 1 MMIO aperture.
18	R/W	0x1	TM_OWNED_DMA	0 = TriMedia does not have access to the DMA MMIO aperture. 1 = TriMedia has access to the DMA MMIO aperture.
17	R/W	0x1	TM_OWNED_TMDBG	0 = TriMedia does not have access to the TriMedia Debug MMIO aperture. 1 = TriMedia has access to the TriMedia Debug MMIO aperture
16	R/W	0x1	TM_OWNED_RESET	0 = TriMedia does not have access to the Reset MMIO aperture. 1 = TriMedia has access to the Reset MMIO aperture.
15	R/W	0x1	TM_OWNED_2D	0 = TriMedia does not have access to the 2D Drawing Engine MMIO aperture. 1 = TriMedia has access to the 2D Drawing Engine MMIO aperture.
14	R/W	0x1	TM_OWNED_MBC	0 = TriMedia does not have access to the M-PI Bus controller MMIO aperture. 1 = TriMedia has access to the M-PI Bus controller MMIO aperture.
13	R/W	0x1	TM_OWNED_GLBREG_2	0 = TriMedia does not have access to Global 2 MMIO aperture. 1 = TriMedia has access to Global 2 MMIO aperture.
12	R/W	0x1	TM_OWNED_UART_3	0 = TriMedia does not have access to the UART3 MMIO aperture. 1 = TriMedia has access to the UART 3 MMIO aperture.
11	R/W	0x1	TM_OWNED_UART_2	0 = TriMedia does not have access to the UART2 MMIO aperture. 1 = TriMedia has access to the UART 2 MMIO aperture.

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GLOBAL 2 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
10	R/W	0x1	TM_OWNED_UART_1	0 = TriMedia does not have access to the UART1 MMIO aperture. 1 = TriMedia has access to the UART1 MMIO aperture.
9	R/W	0x1	TM_OWNED_1394	0 = TriMedia does not have access to the 1394 MMIO aperture. 1 = TriMedia has access to the 1394 MMIO aperture.
8	R/W	0x1	TM_OWNED_USB	0 = TriMedia does not have access to the USB MMIO aperture. 1 = TriMedia has access to the USB MMIO aperture.
7	R/W	0x1	TM_OWNED_CLOCKS	0 = TriMedia does not have access to the Clock MMIO aperture. 1 = TriMedia has access to the Clock MMIO aperture.
6	R/W	0x1	TM_OWNED_I2C_2	0 = TriMedia does not have access to the I2C 2 MMIO aperture. 1 = TriMedia has access to the I2C 2 MMIO aperture.
5	R/W	0x1	TM_OWNED_I2C_1	0 = TriMedia does not have access to the I2C 1 MMIO aperture. 1 = TriMedia has access to the I2C 1 MMIO aperture.
4	R/W	0x1	TM_OWNED_SMARTCARD_2	0 = TriMedia does not have access to Smartcard2 MMIO aperture. 1 = TriMedia has access to the Smartcard2 MMIO aperture.
3	R/W	0x1	TM_OWNED_SMARTCARD_1	0 = TriMedia does not have access to Smartcard1 MMIO aperture. 1 = TriMedia has access to the Smartcard1 MMIO aperture.
2	R/W	0x1	TM_OWNED_BOOT	0 = TriMedia does not have access to the Boot MMIO aperture. 1 = TriMedia has access to the Boot MMIO aperture.
1	R/W	0x1	TM_OWNED_DEBUG	0 = TriMedia does not have access to the Debug MMIO aperture. 1 = TriMedia has access to the Debug MMIO aperture.
0	R/W	0x1	TM_OWNED_PCI_XIO	0 = TriMedia does not have access to the PCI-XIO or PCI-XIO block MMIO apertures. 1 = TriMedia has access to the PCI-XIO and PCI-XIO block MMIO apertures.
Offset 0x04 D004			*TM OWNED T PI*	
31:23		-	Unused	Ignore during writes and read as zeroes.
22	R/W	0x1	TM_OWNED_MSP2	0 = TriMedia does not have access to the MSP2 MMIO aperture. 1 = TriMedia has access to the MSP2 MMIO aperture.
21	R/W	0x1	TM_OWNED_MSP1	0 = TriMedia does not have access to the MSP1 MMIO aperture. 1 = TriMedia has access to the MSP1 MMIO aperture.
20	R/W	0x1	TM_OWNED_TSDMA	0 = TriMedia does not have access to the TSDMA MMIO aperture. 1 = TriMedia has access to the TSDMA MMIO aperture.
19	R/W	0x1	TM_OWNED_AIN3	0 = TriMedia does not have access to the Audio In 3 MMIO aperture. 1 = TriMedia has access to the Audio In 3 MMIO aperture.
18	R/W	0x1	TM_OWNED_AOUT3	0 = TriMedia does not have access to the Audio Out 3 MMIO aperture. 1 = TriMedia has access to the Audio Out 3 MMIO aperture.
17	R/W	0x1	TM_OWNED_AIN2	0 = TriMedia does not have access to the Audio In 2 MMIO aperture. 1 = TriMedia has access to the Audio In 2 MMIO aperture.
16	R/W	0x1	TM_OWNED_AOUT2	0 = TriMedia does not have access to the Audio Out 2 MMIO aperture. 1 = TriMedia has access to the Audio Out 2 MMIO aperture.
15	R/W	0x1	TM_OWNED_AIN1	0 = TriMedia does not have access to the Audio In 1 MMIO aperture. 1 = TriMedia has access to the Audio In 1 MMIO aperture.

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GLOBAL 2 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
14	R/W	0x1	TM_OWNED_AOUT1	0 = TriMedia does not have access to the Audio Out 1 MMIO aperture. 1 = TriMedia has access to the Audio Out 1 MMIO aperture.
13	R/W	0x1	TM_OWNED_AICP2	0 = TriMedia does not have access to the AICP2 MMIO aperture. 1 = TriMedia has access to the AICP2 MMIO aperture.
12	R/W	0x1	TM_OWNED_AICP1	0 = TriMedia does not have access to the AICP1 MMIO aperture. 1 = TriMedia has access to the AICP1 MMIO aperture.
11	R/W	0x1	TM_OWNED_MBS	0 = TriMedia does not have access to the MBS MMIO aperture. 1 = TriMedia has access to the MBS MMIO aperture.
10	R/W	0x1	TM_OWNED_MSP3	0 = TriMedia doesn't have access to the MSP3 MMIO aperture. 1 = TriMedia has access to the MSP3 MMIO aperture.
9	R/W	0x1	TM_OWNED_SPDIFIN	0 = TriMedia does not have access to the SPDIF In MMIO aperture. 1 = TriMedia has access to the SPDIF In MMIO aperture.
8	R/W	0x1	TM_OWNED_SPDIFOUT	0 = TriMedia does not have access to the SPDIF Out MMIO aperture. 1 = TriMedia has access to the SPDIF Out MMIO aperture.
7	R/W	0x1	TM_OWNED_SSI	0 = TriMedia does not have access to the SSI MMIO aperture. 1 = TriMedia has access to the SSI MMIO aperture.
6	R/W	0x1	TM_OWNED_VIP_2	0 = TriMedia does not have access to the VIP2 MMIO aperture. 1 = TriMedia has access to the VIP2 MMIO aperture.
5	R/W	0x1	TM_OWNED_VIP_1	0 = TriMedia does not have access to the VIP1 MMIO aperture. 1 = TriMedia has access to the VIP1 MMIO aperture.
4	R/W	0x1	TM_OWNED_MPG	0 = TriMedia does not have access to the MPEG MMIO aperture. 1 = TriMedia has access to the MPEG MMIO aperture.
3	R/W	0x1	TM_OWNED_GPIO	0 = TriMedia does not have access to the GPIO MMIO aperture. 1 = TriMedia has access to the GPIO MMIO aperture.
2	R/W	0x1	TM_OWNED_TBC	0 = TriMedia does not have access to the T-PI Bus controller MMIO aperture. 1 = TriMedia has access to the T-PI Bus controller MMIO aperture.
1	R/W	0x1	TM_OWNED_TPIC	0 = TriMedia does not have access to TriMedia PIC MMIO aperture. 1 = TriMedia has access to the TriMedia PIC MMIO aperture.
0	R/W	0x1	TM_OWNED_TM32	0 = TriMedia does not have access to the TriMedia MMIO aperture via the PI-Bus. 1 = TriMedia has access to TriMedia MMIO aperture via the PI-Bus.

GLOBAL 2 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
MIPS User Mode Region Registers *(PNX8526 User Manual, Ref. UM10104_1, Chap.2)*				
Offset 0x04 D010			*UM_REGION_LO*	
31:16	R/W	0x0000	UM_REGION_LO	Lowest PI-Bus address mapped to MIPS user mode region, granularity of 64 kB.
15:0		-	Unused	Ignore during writes and read as zeroes.

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GLOBAL 2 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x04 D014			*UM_REGION_HI*	
31:16	R/W	0x0000	UM_REGION_HI	First PI-Bus address outside the MIPS user mode region, granularity of 64 kB. Reset to 0 therefore disabling the MIPS user mode region.
15:0		-	Unused	Ignore during writes and read as zeroes.
TriMedia DRAM Region Registers *(PNX8526 User Manual, Ref. UM10104_1, Chap.2)*				
Offset 0x04 D018			*TM_REGION_LO*	
31:16	R/W	0x0000	TM_REGION_LO	Lowest PI-Bus address that maps to TriMedia and TriMedia-controlled devices in DRAM region, granularity of 64 kB. TM aperture is reset to start at 0.
15:0		-	Unused	Ignore during writes and read as zeroes.
Offset 0x04 D01C			*TM_REGION_HI*	
31:16	R/W	0x0400	TM_REGION_HI	First PI-Bus address outside the TriMedia and TriMedia-controlled devices DRAM region, granularity of 64 kB. TM aperture is reset to 64 MB.
15:0		-	Unused	Ignore during writes and read as zeroes.

GLOBAL 2 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
PCI Inta Output Enable Registers *(PNX8526 User Manual, Ref. UM10104_1, Chaps.6,8)*				
Offset 0x04 D050			*ENABLE_INTA_O*	
31:1		-	Unused	Ignore during writes and read as zeroes.
0	R/W	0x0	ENABLE_INTA_O	Enables PCI INTA output. 0 = Disable PCI inta output. 1 = Enable PCI inta output. Reset is to be disabled.

GLOBAL 2 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
1394 Physical Configuration Register *(PNX8526 User Manual, Ref. UM10104_1, Chap.14)*				
Offset 0x04 D060			*C1394_PHY*	
31:1		-	Unused	Ignore during writes and read as zeroes.
0	R/W	0x0	C1394_PHY	1394 FireWire™ physical configuration 0 = 1394a PHY 1 = 1394-95 Annex J PHY

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GLOBAL 2 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
PI Bridge and PIMI Register *(PNX8526 User Manual, Ref. UM10104_1, Chap.35)*				
Offset 0x04 D100			*MBRIDGE_CTL*	
31:9		-	Unused	Ignore during writes and read as zeroes.
8	R/W	0x0	MPIB_CLKS_SYNC_CF	Clock relationship across the bridge 0 = Clocks are asynchronous. 1 = F-PI to M-PI Bus clock frequency relationship is 2:1.
7	R/W	0x1	MPIB_SEC_PRIORITY_CF	Priority in case of requests from both sides at the same time 0 = F-PI Bus side has priority. 1 = M-PI Bus side has priority. Note: This bit needs to be set to logic 1 in the PNX8526 so that TriMedia can not accept a transaction to its slave MMIO registers while its master is being retracted. To avoid this, the Trimedia side needs priority, which is the M-PI side of the bridge in this case.
6	R/W	0x0	MPIB_BLOCK_ERR_CF	Blocking error acknowledge across the MIPS PI-PI bridge 0 = Do not block error acknowledge. 1 = Block error acknowledge.
5	R/W	0x0	MPIB_POSTED_WRITE_CF	Posted writes 0 = No posting 1 = All writes across bridges are posted writes. (Must be logic 0 for the PNX8526 as posted writes are not supported in the system.)
4:3	R/W	0x3	MPIB_P_RETRACT_CF[1:0]	The bridge can abort an F-PI to M-PI transaction by sending back a retract to the F-PI Bus if it has been waiting too long to get onto the M-PI Bus. The wait time is defined below. 00 = Waits 22 F-PI clock cycles before it retracts. 01 = Waits 43 F-PI clock cycles before it retracts. 10 = Waits 72 F-PI clock cycles before it retracts. 11 = Never retracts.
2:1	R/W	0x3	MPIB_S_RETRACT_CF[1:0]	The bridge can abort an M-PI to F-PI transaction by sending back a retract to the M-PI Bus if it has been waiting too long to get onto the F-PI Bus. The wait time is defined below. 00 = Waits 22 M-PI clock cycles before it retracts. 01 = Waits 43 M-PI clock cycles before it retracts. 10 = Waits 72 M-PI clock cycles before it retracts. 11 = Never retracts.
0	R/W	0x0	MPIB_WINDEBUG_CF	0 = All read types (half word, tri-byte and byte) are not changed by the bridge. 1 = Halfword, tri-byte and byte read transactions on the source side of the bridge are translated into word reads on the target side (for debug only).
Offset 0x04 D104			*FPIMI_CTL*	
31:2		-	Unused	Ignore during writes and read as zeroes.
1	R/W	0x0	FPIMI_POSTED_WRITE	Posted writes 0 = No posting 1 = All writes across the PI to MI gateway are posted writes.
0	R/W	0x0	FPIMI_CLOCKS_ARE_SYNC	Clock relationship across the PI-to-MI gateway 0 = Clocks are asynchronous. 1 = Clocks are synchronous.
Offset 0x04 D108			*MPIMI_CTL*	
31:2		-	Unused	Ignore during writes and read as zeroes.

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GLOBAL 2 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
1	R/W	0x0	MPIMI_POSTED_WRITE	Posted writes 0 = No posting 1 = All writes across the PI-to-MI gateway are posted writes (must be logic zero for the PNX8526).
0	R/W	0x0	MPIMI_CLOCKS_ARE_SYNC	Clock relationship across the PI-to-MI gateway 0 = Clocks are asynchronous. 1 = Clocks are synchronous. (Must be logic 0 for the PNX8526.)
Offset 0x04 D10C			*TPIMI_CTL*	
31:2		-	Unused	Ignore during writes and read as zeroes.
1	R/W	0x0	TPIMI_POSTED_WRITE	Posted writes 0 = No posting 1 = All writes across the PI-to-MI gateway are posted writes. (Must be logic zero for the PNX8526.)
0	R/W	0x0	TPIMI_CLOCKS_ARE_SYNC	Clock relationship across the PI-to-MI gateway 0 = Clocks are asynchronous. 1 = Clocks are synchronous. (Must be logic zero for the PNX8526.)
Offset 0x04 D110			*CBRIDGE_CTL*	
31:9		-	Unused	Ignore during writes and read as zeroes.
8	R/W	0x0	CPIB_CLKS_SYNC_CF	Clock relationship across the bridge 0 = Clocks are asynchronous. 1 = M-PI to T-PI Bus clock frequency relationship is 2:1.
7	R/W	0x1	CPIB_SEC_PRIORITY_CF	Priority in case of requests from both sides at the same time 0 = M-PI Bus side has priority. 1 = T-PI Bus side has priority. Note: This bit needs to be set to logic 1 in the PNX8526 so that TriMedia can not accept a transaction to its slave MMIO registers while its master is being retracted. To avoid this, the Trimedia side needs priority, which is the T-PI side of the bridge in this case.
6	R/W	0x0	CPIB_BLOCK_ERR_CF	Blocking error acknowledge across the cross over PI-PI bridge 0 = Do not block error acknowledge. 1 = Block error acknowledge.
5	R/W	0x0	CPIB_POSTED_WRITE_CF	Posted writes 0 = No posting 1 = All writes across bridges are posted writes. (Must be logic zero for the PNX8526 as posted writes are not supported in the system.)

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GLOBAL 2 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
4:3	R/W	0x0	CPIB_P_RETRACT_CF[1:0]	The bridge can abort an M-PI to T-PI transaction by sending back a retract to the M-PI Bus if it has been waiting too long to get onto the T-PI Bus. The wait time is defined below. 00 = Waits 22 M-PI clock cycles before it retracts. 01 = Waits 43 M-PI clock cycles before it retracts. 10 = Waits 72 M-PI clock cycles before it retracts. 11 = Never retracts.
2:1	R/W	0x0	CPIB_S_RETRACT_CF[1:0]	The bridge can abort a T-PI to M-PI transaction by sending back a retract to the T-PI Bus if it has been waiting too long to get onto the M-PI Bus. The wait time is defined below. 00 = Waits 22 T-PI clock cycles before it retracts. 01 = Waits 43 T-PI clock cycles before it retracts. 10 = Waits 72 T-PI clock cycles before it retracts. 11 = Never retracts.
0	R/W	0x0	CPIB_WINDEBUG_CF	0 = All read types (Halfword, tri-byte and byte) are not changed by the bridge. 1 = Halfword, tri-byte and byte read transactions on the source side of the bridge are translated into word reads on the target side (for debug only).

GLOBAL 2 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
DRAM Location Seen from PI-Bus Registers *(PNX8526 User Manual, Ref. UM10104_1, Chap.2)*				
Offset 0x04 D200			*PI_DRAM_LO*	
31:16	R/W	0x0000	PI_DRAM_LO	Lowest PI-Bus address mapped to DRAM, granularity of 64 kB PI-Bus DRAM aperture is reset to start at 0.
15:0		-	Unused	Ignore during writes and read as zeroes.
Offset 0x04 D204			*PI_DRAM_HI*	
31:16	R/W	0x0400	PI_DRAM_HI	First address outside PI-Bus DRAM space, granularity of 64 kB PI-Bus DRAM aperture is reset to 64 MB.
15:0		-	Unused	Ignore during writes and read as zeroes.

GLOBAL 2 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Transport Stream I/O Register*(PNX8526 User Manual, Ref. UM10104_1, Chap.30)*				
Offset 0x04 D300			*TSIO_REG*	
31:30	R	00	Reserved	
29	R/W	0	TSIN2 mode	Specifies the mode of the interface: 0 = Parallel mode TSIN2 on TSIN21 and TSIN22 1 = Serial mode, TSIN21 and TSIN22 Default = parallel mode

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GLOBAL 2 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
28	R/W	0	TSIN1 mode	Specifies the mode of the interface: 0 = Parallel mode TSIN1 on TSIN11 and TSIN12 1 = Serial mode, TSIN11 and TSIN12 Default = parallel mode
27:26	R	00	Reserved	
25	R/W	0	TSOUT_mode1	TSOUT_mode1: sync style for serial mode 0 = Byte sync 1 = Bit sync Default = byte sync
24	R/W	0	TSOUT_mode0	Specifies the mode of the interface: TSOUT_mode0: 0 = Parallel mode 1 = Serial mode Selection of serial mode enables the parallel to serial conversion. Default = parallel mode
23:20	R/W	0001	MSP3IN_route[3:0]	Specifies the input source for MSP3IN: 0000 = TSIN11 0001 = TSIN12 0010 = TSIN21 0011 = TSIN22 0100 = 1394 RX 0101 = TSDMA others = reserved Default = TSIN12
19:16	R/W	0100	TSOUT_route[3:0]	Specifies the input source for TSOUT: 0100 = 1394 RX 0101 = TSDMA 0110 = MSPOUT1 0111 = MSPOUT2 1000 = MSPOUT3 others = reserved Default = TSIN12
15:12	R/W	0010	TX2_route[3:0]	Specifies the input source for TX2: 0000 = TSIN11 0001 = TSIN12 0010 = TSIN21 0011 = TSIN22 0101 = TSDMA 0110 = MSPOUT1 0111 = MSPOUT2 1000 = MSPOUT3 others = reserved Default = TSIN12

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GLOBAL 2 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
11:8	R/W	0000	TX1_route[3:0]	Specifies the input source for TX1: 0000 = TSIN11 0001 = TSIN12 0010 = TSIN21 0011 = TSIN22 0101 = TSDMA 0110 = MSPOUT1 0111 = MSPOUT2 1000 = MSPOUT3 others = reserved Default = TSIN12
7:4	R/W	0011	MSP2IN_route[3:0]	Specifies the input source for MSP2IN: 0000 = TSIN11 0001 = TSIN12 0010 = TSIN21 0011 = TSIN22 0100 = 1394 RX 0101 = TSDMA others = reserved Default = TSIN12
3:0	R/W	0001	MSP1IN_route[3:0]	Specifies the input source for MSP1IN: 0000 = TSIN11 0001 = TSIN12 0010 = TSIN21 0011 = TSIN22 0100 = 1394 RX 0101 = TSDMA others = reserved Default = TSIN12

GLOBAL 2 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
MMI SDRAM Control Registers *(PNX8526 User Manual, Ref. UM10104_1, Chap.9)*				
Offset 0x04 D400			*MM_SDRAM_SIZE*	
31:2		-	Unused	Ignore during writes and read as zeroes.
1:0	R/W	0x2	MM_SDRAM_SIZE[1:0]	Specifies SDRAM size: 00 = Unused 01 = 16 Mbyte 10 = 32 Mbyte 11 = 64 Mbyte
Offset 0x04 D404			*MM_REFRESH*	
31:10		-	Unused	Ignore during writes and read as zeroes.
9:0	R/W	0x17	MM_REFRESH[9:0]	Refresh period in clock cycles, scaled by 64. Note: This should only be modified when mm_enable=0 and mm_ready=0, then the SDRAM has entered self-refresh and it is safe to change the refresh period.
Offset 0x04 D408			*MM_SHORT_REFRESH*	
31:1		-	Unused	Ignore during writes and read as zeroes.

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GLOBAL 2 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
0	R/W	0x0	MM_SHORT_REFRESH	Short refresh for Quickturn: 0 = Regular refresh 1 = Short refresh
Offset 0x04 D40C			*MM_REFRESH_ENABLED*	
31:1		-	Unused	Ignore during writes and read as zeroes.
0	R/W	0x1	MM_REFRESH_ENABLED	Refresh on or off: 0 = Refresh is off. 1 = Refresh is on.
Offset 0x04 D410			*MM_ENABLE_INTERLEAVE*	
31:1		-	Unused	Ignore during writes and read as zeroes.
0	R/W	0x1	MM_ENABLE_INTERLEAVE	Memory format: 0 = Linear memory format 1 = 2-way interleave memory format
Offset 0x04 D414			*MM_SELF_REFRESH*	
31:3		-	Unused	Ignore during writes and read as zeroes.
2	R/W	0x0	EN_MIPS_COMA_SF	Enable MIPS coma putting SDRAM into self-refresh. 0 = When MIPS goes into coma mode, SDRAM is not put into self-refresh. 1 = When MIPS goes into coma mode, SDRAM is put into self-refresh by MMI (SDRAM memory controller).
1	R	0x1	MM_READY	SDRAM Intialization or powerdown status: 0 = SDRAM is being initialized or in powerdown. 1 = SDRAM intialization is complete and SDRAM is not in powerdown.
0	R/W	0x1	MM_ENABLE	Initialize or powerdown SDRAM: 0 = Powerdown SDRAM. 1 = Functional MMI SDRAM controller
Offset 0x04 D418			*MM_READY_ENABLE*	
31:1		-	Unused	Ignore during writes and read as zeroes.
0	R/W	0x0	MM_READY_ENABLE	Enable write to mm_enable bit not to finish until mm_ready reacts: 0 = Write to mm_enable finishes immediately. 1 = Write to mm_enable bit finishes when mm_ready equals the new value of mm_enable.

GLOBAL 2 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Scratch Registers				
Offset 0x04 D500			*SCRATCH0*	
31:0	R/W	0	SCRATCH0	32-bit writable and readable register
Offset 0x04 D504			*SCRATCH1*	
31:0	R/W	0	SCRATCH1	32-bit writable and readable register
Offset 0x04 D508			*SCRATCH2*	
31:0	R/W	0	SCRATCH2	32-bit writable and readable register

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GLOBAL 2 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x04 D50C			*SCRATCH3*	
31:0	R/W	0	SCRATCH3	32-bit writable and readable register
Offset 0x04 D510			*SCRATCH4*	
31:0	R/W	0	SCRATCH4	32-bit writable and readable register
Offset 0x04 D514			*SCRATCH*	
31:0	R/W	0	SCRATCH5	32-bit writable and readable register
Offset 0x04 D518			*SCRATCH6*	
31:0	R/W	0	SCRATCH6	32-bit writable and readable register
Offset 0x04 D51C			*SCRATCH7*	
31:0	R/W	0	SCRATCH7	32-bit writable and readable register

GLOBAL 2 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
I/O Multiplexer Control Register *(PNX8526 User Manual, Ref. UM10104_1, Chap.35)*				
Offset 0x04 D600			*IO_MUX_CTRL*	
31:15		-	Unused	Ignore during writes and read as zeroes.
14	R/W	0x0	AIO_MUX_SEL	I2S_IO Audio mode: 0 = Select I2S_IO as Audio Out. 1 = Select I2S_IO as Audio In.
13	R/W	0x0	SSI_SEL	SSI or UART3 mode: 0 = Select UART3. 1 = Select SSI.
12	R/W	0x0	RGB24_SEL	Audio Out2 or RGB mode: 0 = Select Audio Out2. 1 = Select RGB (DV_OUT [23:20]).
11:10	R/W	0x0	SMCRD2_MUX_CTRL	ICAM or SmartCard2 mode: 00 = SmartCard1 module ports go to SmartCard2 pins. 01 = SmartCard2 module ports go to SmartCard2 pins. 10 = ICAM1 module ports go to SmartCard2 pins. 11 = ICAM2 module ports go to SmartCard2 pins.
9:8	R/W	0x0	SMCRD1_MUX_CTRL	ICAM or SmartCard2 mode: 00 = SmartCard1 module ports go to SmartCard1 pins. 01 = SmartCard2 module ports go to SmartCard1 pins. 10 = ICAM1 module ports go to SmartCard1 pins. 11 = ICAM2 module ports go to SmartCard1 pins.
7		-	Unused	Ignore during writes and read as zeroes.

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GLOBAL 2 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
6:4	R/W	0x0	VIP2_MUX_CTRL[2:0]	VIP2 module selection: 000 = VIP data from DV1 port 001 = VIP data from DV2 port 010 = VIP data from DV3 port *011 = VIP data from DV_OUT1(AICP1) port *100 = 1394 data from link core *These functions are not available.
3		-	Unused	Ignore during writes and read as zeroes.
2:0	R/W	0x0	VIP1_MUX_CTRL[2:0]	VIP1 module selection: 000 = VIP data from DV1 port 001 = VIP data from DV2 port 010 = VIP data from DV3 port *011 = VIP data from DV_OUT2 (AICP2) port *100 = 1394 data from link core *These functions are not available.

GLOBAL 2 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
TriMedia Powerdown Registers *(PNX8526 User Manual, Ref. UM10104_1, Chap.25)*				
Offset 0x04 D700			*TM32_PWRDWN_REQ*	
31:1		-	Unused	Ignore during writes and read as zeroes.
0	R/W	0x0	TM32_PWRDWN_REQ	TriMedia powerdown request 0 = Do not request a TriMedia powerdown 1 = Request a TriMedia powerdown
Offset 0x04 D704			*TM32_PWRDWN_ACK*	
31:1		-	Unused	Ignore during writes and read as zeroes.
0	R	0x0	TM32_PWRDWN_ACK	0 = Trimedia does not acknowledge powerdown request. 1 = Trimedia acknowledges powerdown request.

GLOBAL 2 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
MMI Arbiter Control Registers For more details on the RAM0—Ram255 registers see *PNX8526 User Manual, Ref. UM10104_1, Chap.36*				
Offset 0x04 D800			*RAM0*	
31:12		-	Unused	Ignore during writes and read as zeroes.
11:8	R/W	NI	Entry1 or Buddy0	In Linear mode, this field = Entry 1 In Buddy mode, this field = Buddy 0
7:4		-	Unused	Ignore during writes and read as zeroes.
3:0	R/W	NI	Entry0 or Primary 0	In Linear mode, this field = Entry 0 In Buddy mode, this field = Primary 0
Offset 0x04 D804			*RAM1*	

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GLOBAL 2 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
31:12		-	Unused	Ignore during writes and read as zeroes.
11:8	R/W	NI	Entry3 or Buddy1	In Linear mode, this field = Entry 3 In Buddy mode, this field = Buddy 1
7:4		-	Unused	Ignore during writes and read as zeroes.
3:0	R/W	NI	Entry2 or Primary1	In Linear mode, this field = Entry 2 In Buddy mode, this field = Primary 1
Offset 0x04 D808			*RAM2*	
31:12		-	Unused	Ignore during writes and read as zeroes.
11:8	R/W	NI	Entry5 or Buddy2	In Linear mode, this field = Entry 5 In Buddy mode, this field = Buddy 2
7:4		-	Unused	Ignore during writes and read as zeroes.
3:0	R/W	NI	Entry4 or Primary2	In Linear mode, this field = Entry 4 In Buddy mode, this field = Primary 2
Offset 0x04 D80C			*RAM3*	
31:12		-	Unused	Ignore during writes and read as zeroes.
11:8	R/W	NI	Entry7 or Buddy3	In Linear mode, this field = Entry 7 In Buddy mode, this field = Buddy 3
7:4		-	Unused	Ignore during writes and read as zeroes.
3:0	R/W	NI	Entry6 or Primary3	In Linear mode, this field = Entry 6 In Buddy mode, this field = Primary 3
Offset 0x04 D810			*RAM4*	
⇓	⇓	⇓	⇓	⇓
Offset 0x04 DBFC			*RAM255*	
31:12		-	Unused	Ignore during writes and read as zeroes.
11:8	R/W	NI	Entry511 or Buddy 255	In Linear mode, this field = Entry 511 In Buddy mode, this field = Buddy 255
7:4		-	Unused	Ignore during writes and read as zeroes.
3:0	R/W	NI	Entry510 or Primary 255	In Linear mode, this field = Entry 510 In Buddy mode, this field = Primary 255
Offset 0x04 DC00			*MODE*	
31:10		-	Unused	Ignore during writes and read as zeroes.
9	R	0x0	ActiveBank	Indicates which ram bank is active. When it is 1, bank A is active. Primarily for diagnostics.
8	R/W	0x0	BankSwitch	Writing a 1 to this register requests a BankSwitch. The hardware automatically clears this register when the BankSwitch is completed.
7		-	Unused	
6	R/W	0x0	delayhunt	When 1, hunting is delayed 2 clocks after the next agent is granted. When 0, the new owner's request signal is masked for 2 clocks after it is granted the bus.
5	R	0x0	dagent1_enabled	Indicates that default_agent1 is enabled in the active bank. Primarily for diagnostics.
4	R	0x0	dagent0_enabled	Indicates that default_agent0 is enabled in the active bank. Primarily for diagnostics.

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GLOBAL 2 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
3	R/W	0x0	buddy	When 1, buddy mode is enabled. When 0, linear mode is enabled. This bit does not become active until the next BankSwitch command is completed.
2	R	-	hunting	A 1 indicates the MMI Arbiter is hunting for the next requesting agent. Primarily for diagnostics.
1	R	0x0	boot_change	A 1 indicates that the Arbiter is changing to/from boot mode. Primarily for diagnostics.
0	R/W	1	boot	Writing a 0 to this bit turns off boot mode. When 1, the arbiter is in boot mode. When 0, the arbiter is in list mode.
Offset 0x04 DC04			*MAXADDR*	
31:8		-	Unused	Ignore during writes and read as zeroes.
7:0	R/W	0x00	MaxAddr	This register specifies the last valid ram address that should be used by the arbiter.
Offset 0x04 DC08			*DEFAULTAGENT0*	
31:8		-	Unused	Ignore during writes and read as zeroes.
7	R/W	0x0	da0_enable	This bit will enable default agent 0 when the bank is made active.
6:4		-	Unused	Ignore during writes and read as zeroes.
3:0	R/W	0x0	dagent0	These bits specify the higher priority default agent.
Offset 0x04 DC0C			*DEFAULTAGENT1*	
31:8		-	Unused	Ignore during writes and read as zeroes.
7	R/W	0x0	da1_enable	This bit will enable default agent 1 when the bank is made active.
6:4		-	Unused	Ignore during writes and read as zeroes.
3:0	R/W	0x0	dagent1	These bits specify the lower priority default agent.

GLOBAL 2 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x04 DFF4			*POWERDOWN*	
31	R/W	0	POWER_DOWN	Powerdown register for the module 0 = Normal operation of the peripheral. This is the reset value. 1 = Module is powered down and module clock can be removed. At powerdown, module responds to all reads with DEADABBA (except for reads of powerdown bit) and all writes with ERR ACK (except for writes to powerdown bit).
30:0		-	Unused	Ignore during writes and read as zeroes.
Offset 0x04 DFFC			*GLB_REG_2_MOD _ID*	
31:16	R	0x0128	MODULE ID	Unique 16-bit code. Module ID 0 and -1 are reserved for future use. This is 0128xH for the Global register 2 module.

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GLOBAL 2 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
15:12	R	1	MAJREV	Major Revision is any revision that might break software compatibility.
11:8	R	0	MINREV	Minor Revision is any revision that maintains software compatibility.
7:0	R	0	MODULE APERTURE SIZE	Aperture size = 4 kB*(bit_value+1). The bit value is reset to 0, which means it is a 4 kB aperture for the Global register 2 module according to this formula.

MPBC Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.35)

M-PI BUS CONTROLLER (MPBC) REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x04 E000			*MPBC_CTRL*	
31:5		-	Unused	Ignore upon read. Write as zeroes.
4:1	R/W	0x0	TOUT_SEL[3:0]	Timeout select 0x0 = Timeout generated after 1 wait cycle. 0x1 = Timeout generated after 3 consecutive wait cycles. 0x2 = Timeout generated after 7 consecutive wait cycles. 0x3 = Timeout generated after 15 consecutive wait cycles. 0x4 = Timeout generated after 31 consecutive wait cycles. 0x5 = Timeout generated after 63 consecutive wait cycles. 0x6 = Timeout generated after 127 consecutive wait cycles. 0x7 = Timeout generated after 255 consecutive wait cycles. 0x8 = Timeout generated after 511 consecutive wait cycles. 0x9 = Timeout generated after 1,023 consecutive wait cycles. 0xa = Timeout generated after 2,047 consecutive wait cycles. 0xb = Timeout generated after 4,095 consecutive wait cycles. 0xc = Timeout generated after 8,191 consecutive wait cycles. 0xd = Timeout generated after 16,383 consecutive wait cycles. 0xe = Timeout generated after 32,767 consecutive wait cycles. 0xf = Timeout generated after 65,535 consecutive wait cycles.
0	R/W	0x1	TOUT_OFF	Timeout disable 0x0 = Timeout enabled. 0x1 = Timeout disabled.
Offset 0x04 E00C			*MPBC_ADDR*	
31:2	R	0x0000 0000-	ERR_TOUT_ADDR[31:2]	Full 30 bits of the M-PI address bus which causes a PI error or timeout.
1:0		-	Unused	Ignore upon read. Write as zeroes.

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M-PI BUS CONTROLLER (MPBC) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x04 E010			*MPBC_STAT*	
31:20	R	0x000	ERR_TOUT_GNT[11:0]	Active master causing error or timeout 0x001 = M-PI Noise generator 0x002 = DMA Engine 0x004 = PCI 0x008 = USB 0x010 = UART 3 0x020 = UART 2 0x040 = UART 1 0x080 = Smartcard 2 0x100 = Smartcard 1 0x200 = Boot 0x400 = MIPS side of C-bridge 0x800 = Peripheral side of M-bridge.
19:18		-	Unused	Ignore upon read. Write as zeroes.
17:12	R	0x00	ERR_TOUT_SEL[5:0]	Selected agent during error or timeout 0x00 = None 0x01 = PCI 0x02 = XIO 0x03 = M-PI to Memory highway bus Interface (M-PIMI) 0x04 = Peripheral side of M-bridge 0x05 = MMIO registers in PCI block 0x06 = Debug 0x07 = Boot 0x08 = Smartcard 1 0x09 = Smartcard 2 0x0a = I2C 1 0x0b = I2C 2 0x0c = Reset 0x0d = USB 0x0e = Link 1394 0x0f = UART 1 0x10 = UART 2 0x11 = UART 3 0x12 = Global register 1 0x13 = M-PI Bus controller 0x14 = 2D Drawing Engine 0x15 = Clock 0x16 = TrIMedia debug 0x17 = DMA 0x18 = Global Register 2 0x19 = MIPS side of C-bridge 0x2a = Null 0x2b = Default slave
11:9		-	Unused	Ignore upon read. Write as zeroes.
8:4	R	0x00	ERR_TOUT_OPC[4:0]	Opcode causing error or timeout. See bits 12:8 of the FPBC_STAT register (offset 0x03_F010) for the Opcode table.
3		-	Unused	Ignore upon read. Write as zeroes.
2:0	R	0x0	ERR_TOUT_ACK[2:0]	Acknowledge during error or timeout. See bits 2:0 of the FPBC_STAT register (offset 0x03_F010) for the ACKs table.
Offset 0x04 E014			*MPBC_MON*	
31:28		-	Unused	Ignore upon read. Write as zeroes.

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M-PI BUS CONTROLLER (MPBC) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
27:16	R	0x000	GNT_LAST[11:0]	Last active master 0x001 = M-PI Noise generator 0x002 = DMA Engine 0x004 = PCI 0x008 = USB 0x010 = UART 3 0x020 = UART 2 0x040 = UART 1 0x080 = Smartcard 2 0x100 = Smartcard 1 0x200 = Boot 0x400 = MIPS side of C-bridge 0x800 = Peripheral side of M-bridge
15:12		-	Unused	Ignore upon read. Write as zeroes.
11:0	R	0x000	REQ_CURR[11:0]	Current requests 0x001 = M-PI Noise generator 0x002 = DMA Engine 0x004 = PCI 0x008 = USB 0x010 = UART 3 0x020 = UART 2 0x040 = UART 1 0x080 = Smartcard 2 0x100 = Smartcard 1 0x200 = Boot 0x400 = MIPS side of C-bridge 0x800 = Peripheral side of M-bridge
Offset 0x04 E01C			*EN_F_PI_APERTURES*	
31:1		-	Unused	Ignore upon read. Write as zeroes.
0	R	0x1	EN_F_PI_APERTURES	Enable F-PI MMIO space to T-PI master registers. 0x0 = Disable F-PI MMIO space to T-PI masters 0x1 = Enable F-PI MMIO space to T-PI masters.
Offset 0x04 EFE0			*MPBC_INT_STATUS*	
31:2			Unused	Ignore upon read. Write as zeroes.
1	R	0	INT_STATUS_TOUT	Timeout interrupt status register. It reports any pending timeout interrupts: 0x1 = Timeout interrupt pending. M-PI Bus controller has generated a timeout because some M-PI device has violated the programmable limit for timeout (see MPBC_TOUT). Or M-bridge or C-bridge generated a timeout request (see PI-PI bridge). 0x0 = Timeout interrupt not pending.
0	R	0	INT_STATUS_ERROR	Error interrupt status register. It reports any pending error interrupts. 0x1 = Error interrupt pending: F-PI Bus controller has detected an error acknowledge on the M-PI Bus. 0x0 = Error interrupt not pending.
Offset 0x04 EFE4			*MPBC_INT_EN*	
31:2		-	Unused	Ignore upon read. Write as zeroes.
1	R/W	0	INT_ENABLE_TOUT	Timeout interrupt enable register 0x1 = Timeout interrupt is enabled. 0x0 = Timeout interrupt is disabled.
0	R/W	0	INT_ENABLE_ERROR	Timeout interrupt enable register 0x1 = Error interrupt is enabled. 0x0 = Error interrupt is disabled.

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M-PI BUS CONTROLLER (MPBC) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x04 EFE8			*MPBC_INT_CLR*	
31:2		-	Unused	Ignore upon read. Write as zeroes.
1	W	0	INT_CLEAR_TOUT	Timeout interrupt clear register. This is written by software to clear the interrupt. 0x1 = Timeout interrupt is cleared. 0x0 = Timeout interrupt is not cleared.
0	W	0	INT_CLEAR_ERROR	Error interrupt clear register. This is written by software to clear the interrupt. 0x1 = Error interrupt is cleared. 0x0 = Error interrupt is not cleared.
Offset 0x04 EFEC			*MPBC_INT_SET*	
31:2		-	Unused	Ignore upon read. Write as zeroes.
1	W	0	INT_SET_TOUT	Timeout interrupt set register. Allows software to set interrupts. 1 = Timeout interrupt is set. 0 = Timeout interrupt is not set.
0	W	0	INT_SET_ERROR	Error interrupt set register. Allows software to set interrupts. 0x1 = Error interrupt is set. 0x0 = Error interrupt is not set.
Offset 0x04 EFFC			*MPBC_MODULE_ID*	
31:16	R	0x010B	MODULE_ID[15:0]	Unique 16-bit code. Module ID 0 and 1 are reserved for future use. Value 0x010B is for the PNX8526 M-PI Bus controller module.
15:12	R	0	MAJREV[3:0]	Major Revision: any revision that might break software compatibility.
11:8	R	1	MINREV[3:0]	Minor Revision: any revision that keeps software compatible.
7:0	R	0	MODULE_APERTURE_SIZE[7:0]	Aperture size = 4kB*(bit_value+1), so 0 means 4kB (the default).

2D Drawing Engine Register

(PNX8526 User Manual, Ref. UM10104_1, Chap.29)

2D DRAWING ENGINE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Drawing Engine Command Registers				
Offset 0x04 F400			*Source Address Base*	
31:29	R/W	0	Swap[2:0]	Specifies endian-swapping on reads from memory. When Swap[2] is 0, swapping is determined by the global endian setting, possibly modified by BSI[0] in EngineConfig. When Swap[2] is 1, swapping is determined by Swap[1:0] as shown: 00=No swapping. Memory is little-endian. 01=Bytes are swapped within each 16-bit word. 10=Words are swapped within each 32-bit double word. 11=Bytes are swapped within each 32-bit double word.
28:24			Reserved	

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2D DRAWING ENGINE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
23:16	R/W	0	Off[22:16]	Specifies the offset for pixel (0,0) of a source bitmap for XY to Linear conversion of addresses. Bits 2:0 must be set to 0.
15:8	R/W	0	Off[15:8]	
7:0	R/W	0	Off[7:0]	
Offset 0x04 F404			*Destination Address Base*	
31:29	R/W	0	Swap[2:0]	Specifies endian-swapping on reads from memory. When Swap[2] is 0, swapping is determined by the global endian setting, possibly modified by BSI[0] in EngineConfig. When Swap[2] is 1, swapping is determined by Swap[1:0] as shown: 00=No swapping. Memory is little-endian. 01=Bytes are swapped within each 16-bit word. 10=Words are swapped within each 32-bit double word. 11=Bytes are swapped within each 32-bit double word.
28:24			Reserved	
23:16	R/W	0	Off[22:16]	Specify the offset for pixel (0,0) of a destination bitmap for XY to Linear conversion of addresses. Bits 2:0 must be set to 0.
15:8	R/W	0	Off[15:8]	
7:0	R/W	0	Off[7:0]	
Offset 0x04 F408			*Pixel Size*	
31:16			Reserved	
15:8	R/W	0	PFormat[7:0]	Currently used only during Alpha-Blending operations. The format is dependent on the color depth. Refer to *PNX8526 User Manual, Ref. UM10104_1, Chap.31* for bit assignments. 16 bpp: 0000_0000 RGB 565 0000_0001 αRGB 4444 0000_0010 RGBα 4534 0000_1000 RGB 565 dithered 0000_1001 αRGB 4444 dithered 0000_1010 RGBα 4534 dithered 32 bpp: 0000_0000 αRGB 8888 0000_0001 αVYU 8888 0000_0010 αYUV 8888 Note: Specifying any other combination of bits will result in an invalid command being executed.
7:0	R/W	0	Depth[5:0]	Specifies the number of bits per pixel. 00100000b 32 bpp 00010000b 16 bpp 00001000b 8 bpp All other values are reserved.
Offset 0x04 F40C			*Source Linear*	
31:24			Reserved	
23:16	R/W	0	Adr[22:16]	Used to load the linear source address for a BLT operation.
15:8	R/W	0	Adr[15:8]	
7:0	R/W	0	Adr[7:0]	
Offset 0x04 F410			*Destination Linear*	
31:24			Reserved	

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2D DRAWING ENGINE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
23:16	R/W	0	Adr[22:16]	Used to load the starting linear pixel address for a vector or the destination linear address for a BLT operation.
15:8	R/W	0	Adr[15:8]	
7:0	R/W	0	Adr[7:0]	
Offset 0x04 F414			*Source Stride*	
31:14			Reserved	
13:0	R/W	0	SrcStr	Used to load the starting linear pixel address for a vector or the destination linear address for a BLT operation. Bits 2:0 must be set to 0.
Offset 0x04 F418			*Destination Stride*	
31:14			Reserved	
13:8	R/W	0	DstStr[13:8]	Hold the offset between adjacent scanlines for BLTs and vectors. Bits 2:0 must be set to 0.
7:0	R/W	0	DstStr[7:0]	
Offset 0x04 F41C			*Color Compare*	
31:24	R/W	0	CCCol[31:24]	Hold the color compare target color.
23:16	R/W	0	CCCol[23:16]	
15:8	R/W	0	CCCol[15:8]	
7:0	R/W	0	CCCol[7:0]	
Offset 0x04 F420			*Mono Host F Color or SurfAlpha*	
31:24	R/W	0	FCol[31:24] alpha[7:0]	Specify the foreground color for host bitmap monochrome expansion. For alpha-blending, this register specifies the global surface alpha values.
23:16	R/W	0	FCol[23:16] R/V/Y[7:0]	
15:8	R/W	0	FCol[15:8] G/Y/U[7:0]	
7:0	R/W	0	FCol[7:0] B/U/V[7:0]	
Offset 0x04 F424			*Mono Host B Color or HAlpha Color*	
31:24	R/W	0	BCol[31:24]	Hold the background color for host bitmap monochrome expansion. For alpha-blending this register may provide color data.
23:16	R/W	0	BCol[23:16] R/V/Y[7:0]	
15:8	R/W	0	BCol[15:8] G/Y/U[7:0]	
7:0	R/W	0	BCol[7:0] B/U/V[7:0]	
Offset 0x04 F428			*Blt Control*	
31:27			Reserved	

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2D DRAWING ENGINE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
26:24	R/W	0	BD[2:0]	The BD[2:0] field specifies the bitblt direction. BD[0] specifies the horizontal BLT direction. It is bit 24 of this register: 0 = Blt direction is left to right. 1 = Blt direction is right to left. BD[1] specifies the vertical BLT direction. It is bit 25 of this register: 0 = Blt direction is top to bottom. 1 = Blt direction is bottom to top. BD[2] enables vertical flipping during the BLT by allowing the source data to be read in the opposite vertical direction from the destination data. Bd[2] is bit 26 of this register: 0 = Src is read as specified in BD[1.] 1 = Src is read in reverse of BD[1].
23:20	R/W	0	A[3:0]	The A[3:0] field controls alpha-blending operations and is in bits 23:20 of this register. A[1:0] controls enabling of alpha-blending and the format of the source data. The valid values are: 0 = Alpha-blending is disabled. 1 = Src data contains normal alpha data. 2 = Src data contains pre-multiplied alpha data. 3 = Src data does not have alpha data, surface alpha is the only alpha value. Bit 2 of this field controls the updating of the alpha field in the destination: 0 = Preserve destination alpha field. 1 = Update destination alpha field. Bit 3 of this field controls whether destination data participates in the alpha blend operation. It is used to implement “unary” blends: 0 = Blend source with destination data 1 = Blend source with black IN RGB mode, “black” means RGB = (0, 0, 0). In YUV mode, “black” means YUV = (16, 128, 128).
19			Reserved	
18:16	R/W	0	CC[2:0]	The CC[2:0] specifies the operation of the color compare hardware. CC[2:0] are bits 19:16 of this register. Legal values are: 0 = Color compare disabled. 1 = SRC data is used for color compare, perform write operation if colors match. 2 = DST data is used for color compare, perform write operation if colors match. 3 = Reserved 4 = Reserved 5 = SRC data is used for color compare, perform write operation if colors don’t match. 6 = DST data is used for color compare, perform write operation if colors don’t match. 7 = Reserved
15:13			Reserved	
12	R/W	0	SP	The SP field indicates if the pattern is a solid color. SP is bit 12 of this register. Legal values are: 0 = Patterns are handled normally. 1 = The value held in the MonoPatFColor foreground color register will be used as pattern data.
11			Reserved	

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2D DRAWING ENGINE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
10:8	R/W	0	SRC[2:0]	The SRC[2:0] field is a 3-bit parameter specifying how the source data are created. SRC[2:0] are in bits 11:8 of this register: 0 = SRC data is color data from SGRAM. This is used for screen-to-screen BLTs with either ROPs or alpha blends. 1 = SRC data is color bitmap data from the host processor. This is used for host-to-screen BLTs with either ROPs or alpha blends. 2 = SRC data is PC mono bitmap data from the host processor. This is used for color expanding host-to-screen BLTs. This encoding implies that host data is padded to a DWORD boundary at the end of scanlines. 3 = SRC data is PC mono font data from the host processor. This is used for text rendering. This encoding implies highly packed host data and forces the Drawing Engine to use SrcStride=BltSize. Width and SrcLinear=0. 4 = SRC data is 4-bit alpha values from the host. This option is used with alpha-blending. 5 = SRC data is 8-bit alpha values from the host. This option is used with alpha-blending. 6 = Use only surface values for alpha-blending, no SRC data present. 7 = Reserved
7:0	R/W	0	ROP[7:0]	The ROP[7:0] field is an 8-bit parameter that specifies the raster op. It is the same format used by GDI. ROP[7:0] are in bits 7:0 of this register.
Offset 0x04 F42C			*Source Address, XY Coordinates*	
31:27			Reserved	
26:24	R/W	0	Y[10:8]	Unsigned 11-bit Y source address
23:16	R/W	0	Y[7:0]	
15:11			Reserved	
10:8	R/W	0	X[10:8]	Unsigned 11-bit X source address
7:0	R/W	0	X[7:0]	
Offset 0x04 F430			*Destination Address, XY Coordinates*	
31:27			Reserved	
26:24	R/W	0	Y[10:8]	Unsigned 11-bit Y destination address
23:16	R/W	0	Y[7:0]	
15:11			Reserved	
10:8	R/W	0	X[10:8]	Unsigned 11-bit X destination address
7:0	R/W	0	X[7:0]	
Offset 0x04 F434			*BLT Size*	
31:28			Reserved	
27:16	R/W	0	H	Height of the BLT in scanlines
15:12			Reserved	
11:0	R/W	0	W	Width of the BLT in pixels
Offset 0x04 F438			*Destination Address, XY2 Coordinates*	
31:27			Reserved	

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2D DRAWING ENGINE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
26:24	R/W	0	Y[10:8]	Unsigned 11-bit Y destination address
23:16	R/W	0	Y[7:0]	
15:11			Reserved	
10:8	R/W	0	X[10:8]	Unsigned 11-bit X destination address
7:0	R/W	0	X[7:0]	
Offset 0x04 F43C			*Vector Constant*	
31:24	R/W	0	Const1 [15:8]	Const1 = 2 x dmin
23:16	R/W	0	Const1 [7:0]	
15:8	R/W	0	Const0 [15:8]	Const0 = 2 x dmin - 2 x dmax
7:0	R/W	0	Const0 [7:0]	
Offset 0x04 F440			*Vector Count Control*	
31:24	R/W	0	InitErr[15:8]	Initial error value for the Bresenham line algorithm
23:16	R/W	0	InitErr[7:0]	
15:8	R/W	0	Oct, Len[11:8]	Bits 15:13 specify the drawing octant as follows: Bit 15 1 Y is major axis 0 X is major axis Bit 14 1 negative X step 0 positive X step Bit 13 1 negative Y step 0 positive Y step
7:0	R/W	0	Len[7:0]	Length of the major axis in pixels
Offset 0x04 F444			*TransMask*	
31:24	R/W	0	TMask[31:24]	Transparency mask used in the color compare
23:16	R/W	0	TMask[23:16]	
15:8	R/W	0	TMask[15:8]	
7:0	R/W	0	TMask[7:0]	
Offset 0x04 F5F8			*MonoPatFColor*	
31:0	R/W	0	MonoPatFColor[31:0]	Specifies the foreground color for monochrome pattern expansion, lines, and solid fills.
Offset 0x04 F5FC			*MonoPatBColor*	
31:0	R/W	0	MonoPatBColor[31:0]	Holds the background color monochrome pattern expansion, lines, and solid fills.

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2D DRAWING ENGINE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Drawing Engine Real Time Registers				
Offset 0x04 F800			*EngineStatus*	
31:11			Reserved	
10	R	0	IRQ	Draw Engine interrupt request status 1 = A 2D interrupt is being requested. This reflects the actual state of the IRQ signal leaving the Drawing Engine.
9	R	0	DEDone	DeDone and DEBusy are the primary Drawing Engine activity indicators.They are the complement of each other. When DEBusy is logic 1 (DEDone a 0), the Drawing Engine is active. If EngineConfig bit 9 is a 1, “active” is defined as: •processing a register access •emptying commands or data from the Host FIFO •performing an operation such as a bitblt or bitblt line •waiting for a memory transaction to complete If EngineConfig bit 9 is a 0, the engine is active when a blt/vector starts and becomes inactive when the blt/vector finishes. All memory writes are complete, AND the host FIFO is empty. DEBusy is read as logic 0, the Drawing Engine is guaranteed to be idle.
8	R	0	DEBusy	
7:4			Reserved	
3	R	0	HFIFO_not empty	Host FIFO is not empty.
2	R	0	HFIFO_full	Host FIFO is full. BLT is busy; another BLT is pending in shadow registers.
1	R	0	Vector active	Vector is in process.
0	R	0	BLT active	BLT is in process.
Offset 0x04 F804			*PanicControl*	
31:8			Reserved	
7:0	W	0	RST	Used to reset the state machines in the Drawing Engine. Writing 0x0000_0001 to this register will halt the Drawing Engine and place it in an idle state. Writing 0x0000_0000 will allow the DE to be reprogrammed and resume normal operation. It may be necessary for software to implement a delay between setting the RST signal to 1 and resetting it to 0.
Offset 0x04 F808			*EngineConfig*	
31:11			Reserved	
10	R/W	0	IRQ_CLR	IRQ_CLR (bit 10) is a self-clearing bit used to reset Drawing Engine IRQ flip-flop. The IRQ flip-flop is set when the DEBusy bit in the EngineStatus register transitions from 1 to 0. It is cleared under software control by setting IRQ_CLR to 1. See BMODE for a description of DEBusy.
9	R/W	0	BMODE	BMODE selects between two slightly different behaviors of DEBusy and DEDone (EngineStatus register). 0=the DEBusy bit is set to 1 when the BLT/vector state machine becomes active i.e., a drawing operation is starting. The bit is cleared only when the state machine is idle, all memory writes are completed, and the command FIFO is empty. 1=the DEBusy bit is set whenever the BLT/vector state machine is active OR the command FIFO is not empty. The DEBusy bit will be cleared when the engine is idle AND the command FIFO is empty. Note that in this mode, the Draw Engine will go busy whenever a register is loaded. Using interrupts can be tricky in this mode.

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2D DRAWING ENGINE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
8	R/W	-	IRQ_EN	IRQ_EN (bit 8) is used to enable the interrupt signal leaving the Drawing Engine module. When IRQ_EN is set to a 1, the interrupt signal is enabled. When set to 0, the interrupt signal leaving the Drawing Engine is masked. The IRQ_EN does not affect the actual IRQ flip-flop. It merely masks the IRQ bit leaving the module.
7:3			Reserved	
2	R/W	0	BSM	BSI (bit 1) and BSM (bit 2) toggle byte and word swapping. Setting BSI to 1 reverses the sense of the global endian bit for data read from the host data input port, so that data are swapped when written when they normally would not be, and vice versa. This bit affects host BLT data, pattern loading. It is intended for debugging and should be set to 0 for normal operation.
1	R/W	0	BSI	BSI (bit 1) and BSM (bit 2) toggle byte and word swapping. Setting BSM to 1 reverses the sense of the global endian bit for data being read and written to the memory port. It is intended for debugging and should be set to 0 for normal operation.
0			Reserved	
Offset 0x04 F80C			*HostFIFOStatus*	
31:6			Reserved	
5:0	R	0	Level[5:0]	Used to provide software with a method of determining the number of available entries in the Host FIFO.
Offset 0x04 FFF4			*POWERDOWN*	
31	R/W	0	POWER_DOWN	Powerdown register for the module 0 = Normal operation of the peripheral. This is the reset value. 1 = Module is powered down and module clock can be removed. At powerdown, module responds to all reads with DEADABBA (except for reads of powerdown bit) and all writes with ERR ACK (except for writes to powerdown bit).
30:0		-	Unused	Ignore during writes and read as zeroes.
Offset 0x04 FFFC			*DeviceID*	
31:16	R	0x0117	ModuleID	ModuleID is 0117h
15:12	R	0	MajRev	The initial Major revision field is 0h.
11:8	R	0	MinRev	The initial Minor revision field is 0h.
7:0	R	0x10	Size	The size is 10h (68 kB).

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2D DRAWING ENGINE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Drawing Engine Data Registers				
Offset 0x04 F600—F6FF			*PatRamMono*	
This address range allows write-only access to the pattern RAM. It is used to load monochrome patterns into the pattern cache with automatic color expansion. Each bit in this address range represents one pixel in the pattern cache. A '1' written here is converted to the foreground color and written to the Pattern RAM. A '0' written here is converted to the background color and written to the Pattern RAM. A monochrome pattern always consists of 64 bits of data regardless of the pixel color depth. The amount of color expanded data, however, is dependent on color depth. The monochrome data should be written to the address range 0x1600 - 0x1607. Note that patterns must be loaded sequentially because the lower order address bits are ignored as a pattern is loaded.				
Offset 0x04 F700—F7FF			*PatRamColor (256 bytes)*	
This address range allows write access to the pattern cache ram. It is only for full color patterns. A full color pattern consists of 64 bytes of data at 8 bpp, 128 bytes at 16 bpp, and 256 bytes of data at 32 bpp. Full color patterns should be loaded starting at address 0x1700. Patterns must be loaded sequentially because the lower order address bits are ignored as a pattern is loaded.				
Offset 0x05 0000—FFFF			*Host Data (64 kB - Memory Space)*	
This address space receives host data for BLTs that require host data. All addresses in this range map to the host write buffer. It allows the host to use REP MOVSD instructions to efficiently copy data from system memory to the BLT engine. When doing a BLT that requires host data (host to screen), it is necessary to program SRC[1:0] in the BltCtl register to select host data. This register is byte accessible, but... Host-to-Screen BLTs always require an integer number of DWORDs to be transferred from the host. Although the HostData port will accept byte writes to load individual bytes of data, writing the high byte actually transfers the host data into the Engine. Reads from this register return unknown data but do not hang the bus. Writing excess data to this register space is not recommended, but will not cause the bus to hang.				

Reset Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.5)

RESET REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x06 0000			*RST_CTL*	
31:6	R/W	-	Unused	
5	R/W	0	sys_big_end	0 = Little-Endian 1 = Big-Endian
4	W	-	Unused	
3	W	NI	rel_mips_rst_n	0 = No action 1 = Release MIPS Reset.
2	W	NI	do_sw_rst	0 = No action 1 = Do Software Reset.
1	W	NI	rel_sys_rst_out	0 = No action 1 = Release System Reset of External Peripherals.
0	W	NI	assert_sys_rst_out	0 = No action 1 = Do System Reset of External Peripherals.
Offset 0x06 0004			*RST_CAUSE*	
Note: This register is set on every write to RST_CTL register or watchdog timeout or reset_in_n.				
31:2		-	Unused	

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RESET REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
1:0	R	NI	RST_CAUSE	Reset Cause register: 00 = Cause is external system reset, reset_in_n. 01 = Cause is software system reset. 11 = Cause is watchdog timeout.
Offset 0x06 0008			*EN_WATCHDOG_RST*	
31:1		-	Unused	
0	R/W	1	EN_WATCHDOG_RST	Enable Watchdog Reset register: 0 = Disable reset due to watchdog timeout. 1 = Enable reset upon watchdog timeout.
Offset 0x06 0FF4			*POWERDOWN*	
31	R/W	0	POWER_DOWN	Powerdown register for the module 0 = Normal operation of the peripheral. This is the reset value. 1 = Module is powered down and module clock can be removed. At powerdown, module responds to all reads with DEADABBA (except for reads of powerdown bit) and all writes with ERR ACK (except for writes to powerdown bit).
30:0		-	Unused	Ignore during writes and read as zeroes.
Offset 0x06 0FFC			*MODULE_ID*	
31:16	R	0x0123	Module_ID	Reset Module ID: 0x0123
15:12	R	0	rev_major	Major revision
11:8	R	0	rev_minor	Minor revision
7:0	R	0	app_size	Aperture size is 0 = 4 kB.

TM32 JTAG S'ware DeBug Port Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.39)

TM32 JTAG SOFTWARE DEBUG PORT REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
TriMedia JTAG Debug Registers				
Offset 0x06 1000			*JTAG_DATA_IN*	
31:0	R/W	0	JTAG_DATA_IN[31:0]	JTAG debugger input data
Offset 0x06 1004			*JTAG_DATA_OUT*	
31:0	R/W	0	JTAG_DATA_OUT[31:0]	JTAG debugger output data
Offset 0x06 1008			*JTAG_CTRL1*	
31:2		-	Unused	
1	R/W	0	sleepless	Set bit to prevent JTAG debug module from going into powerdown.
0	R/W	0	ofull	JTAG output data available handshake bit
Offset 0x06 100C			*JTAG_CTRL2*	
31:1		-	Unused	
0	R/W	0	ifull	JTAG input data available handshake bit

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TM32 JTAG SOFTWARE DEBUG PORT REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x06 1FE0			*Interrupt Status Register*	
31:1		-	Unused	
0	R	0	INTR_STATUS	A logic “1” indicates JTAG interrupt detected.
Offset 0x06 1FE4			*Interrupt Enable Register*	
31:1		-	Unused	
0	R/W	0	INTR_EN	A logic “1” written to a specific bit location will enable the corresponding interrupt in the Interrupt Status register.
Offset 0x06 1FE8			*Interrupt Clear Register*	
31:1		-	Unused	
0	W	0	INTR_CLR	A logic “1” written to a specific bit location will clear the corresponding interrupt in the Interrupt Status register.This bit is self-clearing.
Offset 0x06 1FEC			*Interrupt Set Register*	
31:1		-	Unused	
0	W	0	INTR_SET	A logic “1” written to a specific bit location will set the corresponding interrupt in the Interrupt Status register.
Offset 0x06 1FF4			*Powerdown Register*	
31	R/W	0	POWER_DOWN	JTAG Powerdown indicator 1 = Powerdown 0 = Power up When this bit equals 1, no other registers are accessible.
30:0		-	Unused	
Offset 0x06 1FFC			*Module ID Register*	
31:16	R	0x0127	MOD_ID	JTAG Module ID Number
15:12	R	0	REV_MAJOR	Major revision
11:8	R	0	REV_MINOR	Minor revision
7:0	R	0	APP_SIZE	Aperture size is 0 = 4 kB.

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DMA Controller CRC Checker Register

(PNX8526 User Manual, Ref. UM10104_1, Chap.32)

DMA CONTROLLER AND CRC CHECKER REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x06 2000			*CTL_CNT0*	
31:28	R/W	0	DMACMD	DMA Command Demand Mode: 0100 = MOVE - Move Data 0101 = CRC - Compute CRC Scatter-Gather Mode: 000x = NOP - No data movement. LL_PTR = LL_PTR + 16 x01x = STOP-No data movement. LL_PTR is unchanged. STOP after the current descriptor. 0100 = MOVE - Move Data. LL_PTR = LLPTR + 16 0101 = CRC - Compute CRC. LL_PTR = LL_PTR + 16 x110 = MOVE & STOP - Move Data. LL_PTR is unchanged. STOP after the current descriptor. x111 = CRC & STOP - Compute CRC. LL_PTR is unchanged. STOP after the current descriptor. 100x = JUMP - No data movement. LLPTR = DST_ADDR All other values reserved. (x = “Don’t care.”)
27	R/W	0	LLEN	Link List Enable. (Scatter-Gather Mode (SGM) enable) When this bit is enabled, none of the other bits in this register is affected or changed. Used to support the scatter-gather retrigger mechanism. 0 = SGM transfer off 1 = Start an SGM transfer (reads “SGM transfer in progress”). When this bit is ‘1’, the LL_PTR field must be valid.
26	R/W	0	CHEN	Channel Enable. (Demand Mode (DM) enable) 0 = DM transfer off 1 = Start a DM transfer (reads “DM transfer in progress”). When this bit is ‘1’, the whole channel descriptor must be valid. Note: This bit can be set by the MIPS CPU to start a DMA transfer by loading a descriptor from memory.
25	R/W	0	EOTINTEN	End of Transfer Interrupt Enable. Enables interrupt generation at the end of the current demand-mode transfer. 0 = Disable 1 = Enable
24:23	R/W	0	SRCTYPE	Source Type. Defines the type of the source device: 00 = Memory Device 01 = Reserved 10 = Reserved 11 = Reserved
22	R/W	0	SRCINC	Source Increment. Defines source incrementability: 0 = The Source Address cannot be incremented 1 = The Source Address can be incremented
21:20	R/W	0	DSTTYPE	Destination Type. Defines the type of the destination device: Memory or I/O device width. 00 = Memory Device 01 = 8-bit wide I/O Device (for CRC only) 10 = Reserved 11 = Reserved
19	R/W	0	DSTINC	Destination Increment. Defines destination incrementability: 0 = The Destination Address cannot be incremented. 1 = The Destination Address can be incremented.

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DMA CONTROLLER AND CRC CHECKER REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
18:16	R/W	0	THRCNT	Throttle Count. Sets the threshold limit to the DMA Engine core. 000 = Throttle Disable 001 = 16 bytes 010 = 32 bytes 011 = 48 bytes ... 111 = 112 bytes
15:0	R/W	0	CHAN_CNT	Channel Data Count field is the 16-bit DMA Transfer count. 0 = No transfer 1 to 0xFFFF = Number of bytes of data that will be transferred
Offset 0x06 2004			*SRC_ADDR0*	
31:0	R/W	0	SRC_ADDR	Physical Source Address of the DMA transaction
Offset 0x06 2008			*DST_ADDR0*	
31:0	R/W	0	DST_ADDR	Physical Destination Address of the DMA transaction. For scatter-gather DMA, a new “JUMP” address is stored in this field to reprogram the LL_PTR register.
Offset 0x06 200C			*Reserved*	
Offset 0x06 2010			*Link List Pointer0*	
31:0	R/W	0	LL_PTR	This is the address in memory of the next command descriptor to be fetched and executed (valid only in Scatter-Gather mode).
Offset 0x06 2014—201C			*Reserved*	
Offset 0x06 2020			*CTL_CNT1*	
31:16	R/W	0	CHAN_CTL	Channel Control field that controls the DMA transfer attributes. Refer to the bit description of CTL_CNT0.
15:0	R/W	0	CHAN_CNT	Channel Data Count field is the 16-bit DMA transfer count.
Offset 0x06 2024			*SRC_ADDR1*	
31:0	R/W	0	SRC_ADDR	Physical Source Address of the DMA transaction
Offset 0x06 2028			*DST_ADDR1*	
31:0	R/W	0	DST_ADDR	Physical Destination Address of the DMA transaction. For scatter-gather DMA, a new “JUMP” address is stored in this field to reprogram the LL_PTR register.
Offset 0x06 202C			*Reserved*	
Offset 0x06 2030			*Channel Link List Pointer1*	
31:0	R/W	0	LL_PTR	This is the address in memory of the next descriptor to be fetched and executed (valid only in Scatter-Gather mode).
Offset 0x06 2034—203C			*Reserved*	
Offset 0x06 2040			*CTL_CNT2*	
31:16	R/W	0	CHAN_CTL	Channel Control field that controls the DMA transfer attributes. Refer to the bit description of CTL_CNT0.
15:0	R/W	0	CHAN_CNT	Channel Data Count field is the 16-bit DMA transfer count.
Offset 0x06 2044			*SRC_ADDR2*	
31:0	R/W	0	SRC_ADDR	Physical Source Address of the DMA transaction

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DMA CONTROLLER AND CRC CHECKER REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x06 2048			*DST_ADDR2*	
31:0	R/W	0	DST_ADDR	Physical Destination Address of the DMA transaction. For scatter-gather DMA, a new “JUMP” address is stored in this field to reprogram the LL_PTR register.
Offset 0x06 204C			*Reserved*	
Offset 0x06 2050			*Channel Link List Pointer2*	
31:0	R/W	0	LL_PTR	This is the address in memory of the next descriptor to be fetched and executed (valid only in the Scatter-Gather mode).
Offset 0x06 2054—205C			*Reserved*	
Offset 0x06 2060			*Control and Count Register3 CTL_CNT3*	
31:16	R/W	0	CHAN_CTL	Channel Control field that controls the DMA transfer attributes. Refer to the bit description of CTL_CNT0.
15:0	R/W	0	CHAN_CNT	Channel Data Count field is the 16-bit DMA transfer count.
Offset 0x06 2064			*SRC_ADDR3*	
31:0	R/W	0	SRC_ADDR	Physical Source Address of the DMA transaction
Offset 0x06 2068			*DST_ADDR3*	
31:0	R/W	0	DST_ADDR	Physical Destination Address of the DMA transaction. For scatter-gather DMA, a new “JUMP” address is stored in this field to reprogram the LL_PTR register.
Offset 0x06 206C			*Reserved*	
Offset 0x06 2070			*Channel Link List Pointer3*	
31:0	R/W	0	LL_PTR	This is the address in memory of the next descriptor to be fetched and executed (valid only in the Scatter-Gather mode).
Offset 0x06 2074—207C			*Reserved - For future use (additional channels)*	
Offset 0x06 2080—20FC			*Reserved*	
Offset 0x06 2100			*CRC*	
31:0	R/W	0xFFFF _FFFF	CRC Registers	This register is the CRC accumulator register.
Offset 0x06 2104			*DMA_Control*	
31:9		-	Unused	
8	R/W	0	DMAGEN	DMA Controller Global Enable. Enables/Disables DMA Controller 0 = Disable the DMA Controller centrally, regardless of what other configuration bits are set. 1 = Enables the DMA Controller.
7:4		-	Unused	
3:0	R/W	0	DMACHEN [3:0]	DMA Channel Enable. Selectively enables or disables a particular DMA Channel. Bits 3:0 correspond to DMA channels 3:0. 0 = Disable channel. 1 = Enabled channel.
Offset 0x06 2108—210C			*Reserved*	
Offset 0x06 2110			*DMA Status Register*	
31:4		-	Unused	

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DMA CONTROLLER AND CRC CHECKER REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
3:0	R	0	DMACHBUSY	DMA Channel Busy. Denotes the busy status of the channels. Bits 3:0 correspond to DMA channels 3:0. 0 = Channel is not running. 1 = Channel is busy.
Offset 0x06 2114			*DMA Soft Reset Register*	
31:1		-	Unused	
0	W	0	STBDMA_RST	STB_DMA oft Reset Enable. This register allows software a software reset of the DMA Controller engine. 0 = No Effect. 1 = The DMA Controller is reset by software, except for all the registers and the PI-Bus Interface.
Offset 0x06 2118—23FC			*Reserved*	
Offset 0x06 2FE0			*Interrupt Status Register*	
31:4		-	Unused	
3:0	R	0	STB_DMAINTST	STB_DMA Interrupt Status. This register allows software to check an interrupt status for pending interrupts. Each bit 3:0 reports the status of the corresponding channel interrupt source 3:0. 0 = Interrupt is not pending. 1 = Interrupt is pending. Writing to these bits has no effect.
Offset 0x06 2FE4			*Interrupt Enable Register*	
31:4		-	Unused	
3:0	R/W	0	STB_DMAINTENA	STB_DMA Interrupt Enable. This register allows software to selectively enable an interrupt. Each bit 3:0 controls the corresponding internal interrupt source 3:0. 0 = Interrupt is disabled. 1 = Interrupt is enabled.
Offset 0x06 2FE8			*Interrupt Clear Register*	
31:4		-	Unused	
3:0	W	0	STB_DMAINTCLR	STB_DMA Interrupt Clear. This register allows software to reset an interrupt. Each bit 3:0 controls the corresponding internal interrupt source 3:0. Ignore read data 0 = Interrupt is not cleared. 1 = Interrupt is cleared.
Offset 0x06 2FEC			*Interrupt Set Register*	
31:4		-	Unused	
3:0	W	0	STB_DMAINTSET	STB_DMA Interrupt Set. This register allows software to set an interrupt. Each bit controls each internal interrupt source. Ignore read data 0 = Interrupt is not set. 1 = Interrupt is set.
Offset 0x06 2FF0			*Reserved*	
Offset 0x06 2FF4			*POWERDOWN*	
31	R/W	0	POWER_DOWN	Powerdown register for the module 0 = Normal operation of the peripheral. This is the reset value. 1 = Module is powered down and module clock can be removed. At powerdown, module responds to all reads with DEADABBA (except for reads of powerdown bit) and all writes with ERR ACK (except for writes to powerdown bit).

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DMA CONTROLLER AND CRC CHECKER REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
30:0		-	Unused	Ignore during writes and read as zeroes.
Offset 0x06 2FF8			*Reserved*	
Offset 0x06 2FFC			*Module ID*	
31:16	R	0x0130	MODULEID	STB_DMA Module ID. Returns "0x0130" Writing has no effect.
15:12	R	0	REV_MAJOR	Major revision counter
11:8	R	1	REV_MINOR	Minor revision counter
7:0	R	0	APP_SIZE	Aperture Size 0 = 4kB

Global 1 Registers

GLOBAL 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Scratch Registers				
Offset 0x06 3500			*SCRATCH0*	
31:0	R/W	0	SCRATCH0	32-bit writable and readable register
Offset 0x06 3504			*SCRATCH1*	
31:0	R/W	0	SCRATCH1	32-bit writable and readable register
Offset 0x06 3508			*SCRATCH2*	
31:0	R/W	0	SCRATCH2	32-bit writable and readable register
Offset 0x06 350C			*SCRATCH3*	
31:0	R/W	0	SCRATCH3	32-bit writable and readable register

GLOBAL 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Timer Multiplexer Control Registers *(PNX8526 User Manual, Ref. UM10104_1, Chap.25)*				
Offset 0x06 3704			*TIMER1MUX_CNTL*	
31:4		-	Unused	Ignore during writes and read as zeroes.
3:0	R/W	0x0	TIMER1MUX_CNTL[3:0]	Timer1 input select. 0000 = DV2_CLK (DV2 input clock) 0001 = DV3_CLK (DV3 input clock) 0010 = DV_CLK2 (ICP2 pixel out clock) 0011 = SPDI (from SPDIF In pre-mux "spdi_tstamp") 0100 = I2S_IO_WS (from AIO3 Audio block) 0101 = TS_CLK (Transport Stream Out clock) 0110 = CLK_1394 (1394 master clock) 0111 = SSI_SCLK (external SSI input clock) 1000 = GPIO TIMER1 (source selectable in GPIO block) 1001 = GPIO TIMER2 (source selectable in GPIO block)

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GLOBAL 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x06 3708			*TIMER2MUX_CNTL*	
31:4		-	Unused	Ignore during writes and read as zeroes.
3:0	R/W	0x0	TIMER2MUX_CNTL[3:0]	Timer2 input select. 0000 = DV2_CLK (DV2 input clock) 0001 = DV3_CLK (DV3 input clock) 0010 = DV_CLK2 (ICP2 pixel out clock) 0011 = SPDI (from SPDIF In pre-mux "spdi_tstamp") 0100 = I2S_IO_WS (from AIO3 Audio block) 0101 = TS_CLK (Transport Stream Out clock) 0110 = CLK_1394 (1394 master clock) 0111 = SSI_SCLK (external SSI input clock) 1000 = GPIO TIMER1 (source selectable in GPIO block) 1001 = GPIO TIMER2 (source selectable in GPIO block)
Offset 0x06 370C			*TIMER3MUX_CNTL*	
31:4		-	Unused	Ignore during writes and read as zeroes.
3:0	R/W	0x0	TIMER3MUX_CNTL[3:0]	Timer3 input select. 0000 = DV2_CLK (DV2 input clock) 0001 = DV3_CLK (DV3 input clock) 0010 = DV_CLK2 (ICP2 pixel out clock) 0011 = SPDI (from SPDIF In pre-mux "spdi_tstamp") 0100 = I2S_IO_WS (from AIO3 Audio block) 0101 = TS_CLK (Transport Stream Out clock) 0110 = CLK_1394 (1394 master clock) 0111 = SSI_SCLK (external SSI input clock) 1000 = GPIO TIMER1 (source selectable in GPIO block) 1001 = GPIO TIMER2 (source selectable in GPIO block)
Offset 0x06 3710			*TIMER4MUX_CNTL*	
31:4		-	Unused	Ignore during writes and read as zeroes.
3:0	R/W	0x0	TIMER4MUX_CNTL[3:0]	Timer4 input select. 0000 = DV2_CLK (DV2 input clock) 0001 = DV3_CLK (DV3 input clock) 0010 = DV_CLK2 (ICP2 pixel out clock) 0011 = SPDI (from SPDIF In pre-mux "spdi_tstamp") 0100 = I2S_IO_WS (from AIO3 Audio block) 0101 = TS_CLK (Transport Stream Out clock) 0110 = CLK_1394 (1394 master clock) 0111 = SSI_SCLK (external SSI input clock) 1000 = GPIO TIMER1 (source selectable in GPIO block) 1001 = GPIO TIMER2 (source selectable in GPIO block)

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GLOBAL 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
SPDIF IN Timestamping Register *(PNX8526 User Manual, Ref. UM10104_1, Chap.23)*				
Offset 0x06 3800			*SPDI_MUX_SEL*	
31:4		-	Unused	Ignore during writes and read as zeroes.
3:0	R/W	0x0	SPDI_MUX_SEL	SPDIF IN timestamping. The specific events that may be timestamped are: 0000 = WS - Word strobe 0001 = SWS - Last subframe 0010 = SPDI_STATUS[0] - Buffer 1 full 0011 = SPDI_STATUS[1] - Buffer 2 full 0100 = SPDI_STATUS[2] - Buffer 1 active 0101 = SPDI_STATUS[3] - Bandwidth Error 0110 = SPDI_STATUS[4] - Parity Error 0111 = SPDI_STATUS[5] - Validity Error 1000 = SPDI_STATUS[6] - User/Channel bits available 1001 = SPDI_STATUS[7] - Unlock active

GLOBAL 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x06 3FF4			*POWERDOWN*	
31	R/W	0	POWER_DOWN	Powerdown register for the module 0 = Normal operation of the peripheral. This is the reset value. 1 = Module is powered down and module clock can be removed. At powerdown, module responds to all reads with DEADABBA (except for reads of powerdown bit) and all writes with ERR ACK (except for writes to powerdown bit).
30:0		-	Unused	Ignore during writes and read as zeroes.
Offset 0x06 3FFC			*GLB_REG_1_MOD _ID*	
31:8	R	0x0126	MODULE ID	Unique 16-bit code. Module ID 0 and -1 are reserved for future use. This is 0126xH for the Global register1 module.
15:12	R	0	MAJREV	Major Revision is any revision that might break software compatibility.
11:8	R	0	MINREV	Minor Revision is any revision that maintains software compatibility.
7:0	R	0	MODULE APERTURE SIZE	Aperture size = 4 kB*(bit_value+1). The bit value is reset to 0, which means it is a 4 kB aperture for the Global register 1 module according to the formula above.

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MPI Null Module Registers

MPI NULL MODULE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x06 4FFC			*Module ID Register*	
31:16	R	0x0124	MOD_ID	Module ID Number
15:12	R	0	REV_MAJOR	Major revision
11:8	R	0	REV_MINOR	Minor revision
7:0	R	0x9B	APP_SIZE	Aperture size is 0 = 4 kB.

TM32 CPU Core Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.25)

TM32 CPU CORE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Cache and Memory System				
Offset 0x10 000C			*MEM_EVENTS*	
31:8		-	Unused	
7:4	R/W	0	Event2	Selects the source for TM32 CPU TIMER CACHE2 event: 0 = No event 1 = Instruction Cache Misses 2 = Instruction Cache stall cycles (includes cycles where I and Dcache both stall) 3 = Data Cache Bank Conflicts 4 = Data Cache Read Misses 5 = Data Cache Write Misses 6 = Data Cache stall cycles (excludes cycles where I and D cache both stall) 7 = Data Cache Copybacks to SDRAM 8 = Copyback Buffer Full 9 = Data cache write miss with all fetch units occupied 10 = Data Cache stream miss 11 = Prefetch Operation Started and not discarded 12 = Prefetch Operation Discarded (already in Dcache, or no fetch unit) 13 = Prefetch Operation Discarded (already in Dcache) 14, 15 = RESERVED
3:0	R/W	0	Event1	Selects the source for TM32 CPU TIMER CACHE1 event.
Offset 0x10 0010			*DC_LOCK_CTL*	
31:1		-	Unused	

TM32 CPU CORE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
0	R/W	0	DC_LOCK_ENABLE	0 = Disable Data Cache Locking 1 = Enable locking for all bytes in the range DC_LOCK_ADDRESS <= a <= DC_LOCK_ADDRESS + DC_LOCK_SIZE -1, and bring this data in from main memory.
Offset 0x10 0014			*DC_LOCK_ADDR*	
31:14	R/W	0	DC_LOCK_ADDRESS[31:14]	Lower bound of memory byte address range that becomes data cache locked when DC_LOCK_ENABLE is asserted. The full range is DC_LOCK_ADDRESS <= a <= DC_LOCK_ADDRESS + DC_LOCK_SIZE -1.
13:0	R	0	DC_LOCK_ADDRESS[13:0]	These bits of DC_LOCK_ADDRESS must be zero due to alignment restrictions for the locked range.
Offset 0x10 0018			*DC-LOCK_SIZE*	
31:13		0	Unused	
12:6	R/W	0	DC_LOCK_SIZE[12:6]	Size of memory byte address range that becomes data cache locked when DC_LOCK_ENABLE is asserted. The full range is DC_LOCK_ADDRESS <= a <= DC_LOCK_ADDRESS + DC_LOCK_SIZE -1.
5:0	R	0	DC_LOCK_SIZE[5:0]	These bits must be 0 due to locked address range alignment restrictions
Offset 0x10 001C			*DC_PARAMS*	
31:26			Reserved	
25:16	R	64	BLOCKSIZE	Block Size of Data Cache, in bytes
15:11	R	8	ASSOCIATIVITY	Associativity of Data Cache
10:0	R	32	NUMBER_OF_SETS	Number of sets in Data Cache
Offset 0x10 0020			*IC_PARAMS*	
31:26			Reserved	
25:16	R	64	BLOCKSIZE	Block Size of Instruction Cache, in bytes
15:11	R	8	ASSOCIATIVITY	Associativity of Instruction Cache
10:0	R	64	NUMBER_OF_SETS	Number of sets in Instruction Cache

TM32 CPU CORE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
TM32 Control and Status Registers				
Offset 0x10 0030			*TM32_CTL*	
The TM32_CTL register is not writable by the TM32 CPU core.				
31:30	W	NI	ACTION	00 = no action 01 = stop and reset TM32 CPU core immediately. 10 = start TM32 CPU core (execution starts at TM32_START_ADR). 11 = Reserved
29:7		-	Unused	

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TM32 CPU CORE REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
6	R/W	0x1	PLL_EN	1 = PLL is generating the TM32 CPU core internal clock. 0 = PLL is disabled. Take TM32 CPU core internal clock directly from clk_tm32 core input, i.e. SDRAM_CLK in PNX8525.
5:0	R/W	0x9	RATIO	TM32 CPU core speed to clk_tm32 core input clock ratio 001001 = 1.0 (Note: In 1.0 RATIO, PLL_EN should be set to 0, i.e., the internal PLL should not be enabled.) 101100 = 1.25 100011 = 1.3333333 111101 = 1.4 011010 = 1.50 101011 = 1.6666666 111100 = 1.75 010001 = 2.0 Other = Reserved
This register allows the on-chip MIPS CPU, an external PCI host CPU, or any other PI-Bus master to STOP or START the TM32 CPU core and to set its operating frequency. Upon START, the TM32 CPU core starts execution from the address in the TM32_START_ADR MMIO register. Note that RATIO should only be changed while the TM32 CPU is stopped. After changing RATIO, a period of 1 µs delay should be taken before performing a TM32 CPU core start.				
Offset 0x10 0034			*TM32_DRAM_LO*	
The TM32_DRAM_LO register is not writable by the TM32 CPU core.				
31:16	R/W	0x0000	TM32_DRAM_LO[31:16]	The TM32 CPU core goes out across the DVP memory bus for all loads/stores with TM32_DRAM_LO <= a < TM32_DRAM_HI
15:0	R	0x0000	TM32_DRAM_LO[15:0]	Must be zeroes due to 64 kB address alignment requirement
The TM32 CPU core is restricted to DRAM accesses from the 32-bit address TM32_DRAM_LO...TM32_DRAM_HI-1. During system boot and configuration, the values of TM32_DRAM_LO and TM32_DRAM_HI are set by the host CPU or the Boot block. The TM32 CPU core can read the values, but not change them. This prevents accidental or intentional overwriting of critical system data in DRAM, such as MIPS kernel data structures.				
Offset 0x10 0038			*TM32_DRAM_HI*	
The TM32_DRAM_HI register is not writable by the TM32 CPU core.				
31:16	R/W	0x0100	TM32_DRAM_HI[31:16]	This register is the highest DRAM address that TM32 CPU core can access. See register TM32_DRAM_LO for more details.
15:0	R	0x0000	TM32_DRAM_HI[15:0]	Must be zeroes due to 64 kB address alignment requirement
Offset 0x10 003C			*TM32_DRAM_CLIMIT*	
The TM32_DRAM_CLIMIT register is not writable by the TM32 CPU core. NOTE: this restriction may be removed in future implementations of the TM32 CPU core.				
31:16	R/W	0x00ff	TM32_DRAM_CLIMIT[31:16]	TM32 CPU.Dcache is allowed to cache DRAM accesses from TM32_DRAM_LO...TM32_DRAM_CLIMIT-1. Addresses from TM32_DRAM_CLIMIT...TM32_DRAM_HI-1 are non-cached.
15:0	R	0x0000	TM32_DRAM_CLIMIT[15:0]	Must be zeroes due to 64 kB address alignment requirement
Offset 0x10 0040			*TM32_APERT1_LO*	
The TM32_APERT1_LO register is not writable by the TM32 CPU core.				
31:16	R/W	0x1c00	TM32_APERT1_LO[31:16]	Lowest TM32 CPU core address that resolves to a PI access.
15:0	R	0x0000	TM32_APERT1_LO[15:0]	Must be zeroes due to 64 kB address alignment requirement
Any TM32 CPU core data access that falls between TM32_APERT1_LO...TM32_APERT1_HI-1 is resolved to a PI-Bus access. This aperture is intended to be mapped on the XIO bus to allow TriMedia to execute from Flash and access selected XIO peripherals. But it can be used for other purposes. There is no built-in interpretation of the aperture structure, size or position.				

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TM32 CPU CORE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 0044			*TM32_APERT1_HI*	
The TM32_APERT1_HI register is not writable by the TM32 CPU core.				
31:16	R/W	0x2000	TM32_APERT1_HI[31:16]	TM32_APERT1_HI-1 is the highest TM32 CPU core address that resolves to a PI access. See register TM32_APERT1_LO for more details.
15:0	R	0x0000	TM32_APERT1_HI[15:0]	Must be zeroes due to 64 kB address alignment requirement
Offset 0x10 0048			*TM32_START_ADR*	
The TM32_START_ADR register is not writable by the TM32 CPU core.				
31:6	R/W	0x0	TM32_START_ADR[31:6]	PC start value for TM32 CPU core upon start of execution. Must be 64 byte aligned.
5:0	R	0x0	TM32_START_ADR[5:0]	Must be zeroes due to 64 byte alignment restriction
This MMIO register should be given a defined value before performing a TM32 CPU core 'start' by writing to TM32_CTL.ACTION. The value in TM32_START_ADR should lie inside TM32_DRAM_LO...TM32_DRAM_HI-1. This register should only be written to while the TM32 CPU core is in the stopped state.				
Offset 0x10 004C			*TM32_PC*	
31:0	R	NI	n/a	PC value of TM32 CPU core
This read-only register reflects the instantaneous value of the TM32 CPU core program counter. It can be read by any PI-Bus master, as well as by the TM32 CPU core itself. When read by the TM32 CPU core using 32-bit load operations, the value returned is precisely defined as the address of the VLIW instruction containing the load operation.				

TM32 CPU CORE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Partial Powerdown				
Offset 0x10 0108			*POWER_DOWN*	
This register should only be written by the TM32 CPU core, to perform a voluntary powerdown. The effect of externally initiated writes to this register is undefined!				
31:0	W			A TM32 CPU write to this register initiates a voluntary powerdown of the TM32 CPU. Execution continues where it left off upon any non-masked interrupt to the TM32 CPU core, or upon any incoming PI-bus MMIO write to the TM32 CPU.
Instruction Cache Locking				
Offset 0x10 0210			*IC_LOCK_CTL*	
31:1		-	Unused	
0	R/W	0	IC_LOCK_ENABLE	0 = Instruction Cache Locking is disabled 1 = Enable locking for addresses in the range IC_LOCK_ADDR <= a <= IC_LOCK_ADDR + IC_LOCK_SIZE -1, and bring all instructions in this range into the Icache.
Offset 0x10 0214			*IC_LOCK_ADDR*	
31:15	R/W	0	IC_LOCK_ADDRESS[31:15]	Lower bound of memory byte address range that becomes instruction cache locked when IC_LOCK_ENABLE is asserted. The full range is IC_LOCK_ADDRESS <= a <= IC_LOCK_ADDRESS + IC_LOCK_SIZE -1.
14:0	R	0	IC_LOCK_ADDRESS[14:0]	Must be all zeroes due to alignment restrictions

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TM32 CPU CORE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 0218			*IC_LOCK_SIZE*	
31:14		-	Unused	
13:6	R/W	0	IC_LOCK_SIZE[13:6]	Size of memory byte address range that becomes instruction cache locked when IC_LOCK_ENABLE is asserted. The full range is IC_LOCK_ADDRESS <= a <= IC_LOCK_ADDRESS + IC_LOCK_SIZE -1.
5:0	R	0	IC_LOCK_SIZE[5:0]	Must be all zeroes due to alignment restrictions

TM32 CPU CORE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Miscellaneous Registers				
Offset 0x10 0500			*SEM*	
31:12		-	Unused	
11:0	R/W	0	SEM	Multi-Processor Semaphore assist device. Writing a zero to this field makes the field zero Writing a non-zero to this field succeeds if and only if the field was zero

TM32 CPU CORE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Exception and Interrupt Control and Vectors				
Offset 0x10 0800			*EXCVEC*	
31:0	R/W	0	Exception Vector	Address of exception handler routine.
Offset 0x10 0810			*ISETTING0*	
Interrupt Mode and Priority for sources 0..7				
31:28	R/W	0	MP7	Each MP Field [xxxx]: 0xxx: source operates in edge-triggered mode. 1xxx: source operates in level-sensitive mode. Each MP Field [xxxx]: x111 NMI (highest) priority x110 maskable level 6 ... x000 maskable level 0
27:24	R/W	0	MP6	
23:20	R/W	0	MP5	
19:16	R/W	0	MP4	
15:12	R/W	0	MP3	
11:8	R/W	0	MP2	
7:4	R/W	0	MP1	
3:0	R/W	0	MP0	

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TM32 CPU CORE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 0814			*ISETTING1*	
Interrupt Mode and Priority for sources 8..15				
31:28	R/W	0	MP15	Each MP Field [xxxx]: 0xxx: source operates in edge-triggered mode. 1xxx: source operates in level-sensitive mode. Each MP Field [xxxx]: x111 NMI (highest) priority x110 maskable level 6 ... x000 maskable level 0
27:24	R/W	0	MP14	
23:20	R/W	0	MP13	
19:16	R/W	0	MP12	
15:12	R/W	0	MP11	
11:8	R/W	0	MP10	
7:4	R/W	0	MP9	
3:0	R/W	0	MP8	
Offset 0x10 0818			*ISETTING2*	
Interrupt Mode and Priority for sources 16..23				
31:28	R/W	0	MP23	Each MP Field [xxxx]: 0xxx: source operates in edge-triggered mode. 1xxx: source operates in level-sensitive mode. Each MP Field [xxxx]: x111 NMI (highest) priority x110 maskable level 6 ... x000 maskable level 0
27:24	R/W	0	MP22	
23:20	R/W	0	MP21	
19:16	R/W	0	MP20	
15:12	R/W	0	MP19	
11:8	R/W	0	MP18	
7:4	R/W	0	MP17	
3:0	R/W	0	MP16	
Offset 0x10 081C			*ISETTING3*	
Interrupt Mode and Priority for sources 24..31				
31:28	R/W	0	MP31	Each MP Field [xxxx]: 0xxx: source operates in edge-triggered mode. 1xxx: source operates in level-sensitive mode. Each MP Field [xxxx]: x111 NMI (highest) priority x110 maskable level 6 ... x000 maskable level 0
27:24	R/W	0	MP30	
23:20	R/W	0	MP29	
19:16	R/W	0	MP28	
15:12	R/W	0	MP27	
11:8	R/W	0	MP26	
7:4	R/W	0	MP25	
3:0	R/W	0	MP24	
Interrupt Controller Request, Clear and Mask MMIO				
Offset 0x10 0820			*IPENDING*	
31:0	R/W	0	IPENDING	Each IPENDING(i) bit: On read, 1=source i interrupt request is currently pending. On write, 1=assert source i interrupt request. Note: Functionality of this register may be affected by other TM32 registers.

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TM32 CPU CORE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 0824			*ICLEAR*	
31:0	R/W	0	ICLEAR	Each ICLEAR(i) bit: On read, same as IPENDING(i) On write, 1=clear source i interrupt request Note: Functionality of this register may be affected by other TM32 registers.
Offset 0x10 0828			*IMASK*	
31:0	R/W	0	IMASK	Each IMASK(*i*) bit: On read or write, 0=disallow source *i* interrupt request. On read or write, 1=allow source *i* interrupt request.
Offset 0x10 0880			*INTVEC0*	
31:0	R/W	NI	Source 0 vector	Address of interrupt handler routine for source 0
Offset 0x10 0884			*INTVEC1*	
31:0	R/W	NI	Source 1 vector	Address of interrupt handler routine for source 1
Offset 0x10 0888			*INTVEC2*	
31:0	R/W	NI	Source 2 vector	Address of interrupt handler routine for source 2
⇓	⇓	⇓	⇓	⇓
Offset 0x10 08F8			*INTVEC30*	
31:0	R/W	NI	Source 30 vector	Address of interrupt handler routine for source 30
Offset 0x10 08FC			*INTVEC31*	
31:0	R/W	NI	Source 31 vector	Address of interrupt handler routine for source 31

TM32 CPU CORE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
CPU Timers/Counters				
Offset 0x10 0C00			*TIMER1_TMODULUS*	
31:0	R/W	NI	TMODULUS	Timer Modulus value. When the Timer reaches this value it wraps around to 0 (or to 1 in the case of increment by 2).
Offset 0x10 0C04			*TIMER1_TVALUE*	
31:0	R/W	NI	TVALUE	Timer Value
Offset 0x10 0C08			*TIMER1_TCTL*	
31:20		-	Unused	
19:16	R/W	0	PRESCALE	Prescale value is 2^PRESCALE, i.e., in the range [1..32768]
15:12		-	Unused	

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TM32 CPU CORE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
11:8	R/W	0	SOURCE	Timer Source select: 0 = TM32 CPU clock 1 = pre-scaled CPU clock 2 = TIMERMUX1 external expansion mux 3 = data breakpoints 4 = instruction breakpoints 5 = cache event 1 6 = cache event 2 7 = DV1_CLK (DV1 input clock) 8 = DV_CLK1 (AICP1 output clock) 9 = Audio In 1 word strobe 10 = Audio Out 1 word strobe 11 = do not use 12 = do not use 13 = do not use 14 = Audio In 2 word strobe 15 = Audio Out 2 word strobe
7:1		-	Unused	
0	R/W	0	RUN	“RUN” bit: 0 = Timer1 stopped 1 = Timer1 running
Offset 0x10 0C20			*TIMER2_TMODULUS*	
31:0	R/W	NI	TMODULUS	Timer Modulus value. When the Timer reaches this value it wraps around to 0 (or to 1 in the case of increment by 2).
Offset 0x10 0C24			*TIMER2_TVALUE*	
31:0	R/W	NI	TVALUE	Timer Value
Offset 0x10 0C28			*TIMER2_TCTL*	
31:20		-	Unused	
19:16	R/W	0	PRESCALE	Prescale value is 2^PRESCALE, i.e., in the range [1..32768]
15:12		-	Unused	
11:8	R/W	0	SOURCE	Timer Source select: 0 = TM32 CPU clock 1 = pre-scaled CPU clock 2 = do not use 3 = data breakpoints 4 = instruction breakpoints 5 = cache event 1 6 = cache event 2 7 = DV1_CLK (DV1 input clock) 8 = DV_CLK1 (AICP1 output clock) 9 = Audio In 1 word strobe 10 = Audio Out 1 word strobe 11 = TIMER2MUX external expansion mux 12 = do not use 13 = do not use 14 = Audio In 2 word strobe 15 = Audio Out 2 word strobe
7:1		-	Unused	
0	R/W	0	RUN	“RUN” bit: 0 = Timer2 stopped 1 = Timer2 running

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TM32 CPU CORE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 0C40			*TIMER3_TMODULUS*	
31:0	R/W	NI	TMODULUS	Timer Modulus value. When the Timer reaches this value it wraps around to 0 (or to 1 in the case of increment by 2).
Offset 0x10 0C44			*TIMER3_TVALUE*	
31:0	R/W	NI	TVALUE	Timer Value
Offset 0x10 0C48			*TIMER3_TCTL*	
31:20		-	Unused	
19:16	R/W	0	PRESCALE	Prescale value is 2^PRESCALE, i.e., in the range [1..32768]
15:12		-	Unused	
11:8	R/W	0	SOURCE	Timer Source select: 0 = TM32 CPU clock 1 = pre-scaled CPU clock 2 = do not use 3 = data breakpoints 4 = instruction breakpoints 5 = cache event 1 6 = cache event 2 7 = DV1_CLK (DV1 input clock) 8 = DV_CLK1 (AICP1 output clock) 9 = Audio In 1 word strobe 10 = Audio Out 1 word strobe 11 = do not use 12 = TIMER3MUX external expansion mux 13 = do not use 14 = Audio In 2 word strobe 15 = Audio Out 2 word strobe
7:1		-	Unused	
0	R/W	0	RUN	“RUN” bit: 0 = Timer3 stopped 1 = Timer3 running
Offset 0x10 0C60			*SYSTIMER_TMODULUS*	
31:0	R/W	NI	TMODULUS	Timer Modulus value. When the Timer reaches this value it wraps around to 0 (or to 1 in the case of increment by 2).
Offset 0x10 0C64			*SYSTIMER_TVALUE*	
31:0	R/W	NI	TVALUE	Timer Value
Offset 0x10 0C68			*SYSTIMER_TCTL*	
31:20		-	Unused	
19:16	R/W	0	PRESCALE	Prescale value is 2^PRESCALE, i.e., in the range [1..32768]
15:12		-	Unused	

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TM32 CPU CORE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
11:8	R/W	0	SOURCE	Timer Source select: 0 = TM32 CPU clock 1 = pre-scaled CPU clock 2 = do not use 3 = data breakpoints 4 = instruction breakpoints 5 = cache event 1 6 = cache event 2 7 = DV1_CLK (DV1 input clock) 8 = DV_CLK1 (AICP1 output clock) 9 = Audio In 1 word strobe 10 = Audio Out 1 word strobe 11 = do not use 12 = do not use 13 = TIMER4MUX external expansion mux 14 = Audio In 2 word strobe 15 = Audio Out 2 word strobe
7:1		-	Unused	
0	R/W	0	RUN	"RUN" bit: 0 = SysTimer stopped 1 = SysTimer running

TM32 CPU CORE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Nexperia Module ID				
Offset 0x10 0FFC			*TM32_MODID*	
31:16	R	0x2B80	Module	Module Code 0x2b80 designates TM32 CPU core
15:12	R	0	Major rev	Major design revision number of core
11:8	R	0	Minor rev	Minor design rev number (metal update)
7:0	R	0x01	Aperture size	MMIO Aperture size code = 8 kB

TM32 CPU CORE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Instruction Breakpoint Control and Address Range Registers				
Offset 0x10 1000			*BICTL*	
31:9		-	Unused	
8	R/W	0	IAC	Instruction Address breakpoint Control 0 = Breakpoint if BINSTLOW <= addr <= BINSTHIGH 1 = Breakpoint if addr < BINSTLOW or addr > BINSTHIGH
7:1		-	Unused	

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TM32 CPU CORE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
0	R/W	0	IC	"IC" Instruction breakpoint Control bit: 0 = Disable instruction breakpoints. 1 = Enable instruction breakpoints.
Offset 0x10 1004			*BINSTLOW*	
31:0	R/W	0	BINSTLOW	Instruction Breakpoint Range Low Address
Offset 0x10 1008			*BINSTHIGH*	
31:0	R/W	0	BINSTHIGH	Instruction Breakpoint Range High Address

TM32 CPU CORE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Data Breakpoint Control Registers				
Offset 0x10 1020			*BDCTL*	
31:17		-	Unused	
16	R/W	0	DVC	Control field for data breakpoints: 0 = Break if data (under BDATAMASK) equal BDATAVAL 1 = Break if data (under BDATAMASK) not equal BDATAVAL
15:9		-	Unused	
8	R/W	0	DAC	"DAC" Data Address Control: 0 = Break if BDATALOW <= addr <= BDATAHIGH 1 = Break if addr < BDATALOW or addr >= BDATAHIGH
7:4		-	Unused	
3	R/W	0	BS	"BS" Break on Store: 0 = Don't check data stores. 1 = Do check data stores.
2	R/W	0	BL	"BL" Break on Load: 0 = Don't check data loads. 1 = Do check data loads.
1:0	R/W	0	DC	"DC" Data Control: 0 = Disable Data Breakpoints 1 = Enable break on data addresses only 2 = Enable break on data values only 3 = Enable break only when both address and value meet conditions
Data Breakpoint Address Range and Value Compare Registers				
Offset 0x10 1030			*BDATAALOW*	
31:0	R/W	0	BDATAALOW	Address Range Start
Offset 0x10 1034			*BDATAAHIGH*	
31:0	R/W	0	BDATAAHIGH	Address Range End

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TM32 CPU CORE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 1038			*BDATAVAL*	
31:0	R/W	0	BDATAVAL	Data Breakpoint Value
Offset 0x10 103C			*BDATAMASK*	
31:0	R/W	0	BDATAMASK	Data Breakpoint Value Mask - only bits that are '1' are taken into account when doing the data breakpoint value compare (for equal or non-equal). Use a nonzero value in this field when enabling data value breakpoints.

T-PIC Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.6)

PRIORITY INTERRUPT CONTROLLER (T-PIC) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 2000			*PIC_INT_PRIORITY*	
31:4		-	Unused	Read as zero
3:0	R/W	0xF	PRIORITY_LIMITER	Interrupt Priority Limiter: Pending Interrupts with priority greater than the PRIORITY_ LIMITER raise an interrupt to the CPU. Special case: PRIORITY_LIMITER = 15 No interrupts can be raised to the CPU via the CPUINT, only CPUNMI can be generated.
Offset 0x10 2004			*PIC_INT_SRC*	
31:12	R/W	0	INT_TABLE_ADDR	Base address for Interrupt Handlers address table. Interrupt Handler routines address table is 4096 byte-aligned in memory at this location.
11:3	R	0	INT_SRC	Interrupt Source. This field identifies the highest priority pending interrupt at the time this register was read. This allows room for 511 interrupt sources. Value 0 indicates no pending interrupt.
2:0		-	Unused	Read as zero.
Offset 0x10 2008—2010			*Reserved*	
Offset 0x10 2014			*PIC_INT_REG_1*	
31	R	NI	INT_PENDING	Interrupt Pending Reads to this register indicate whether the interrupt is pending for service regardless of the INT_PRIORITY value and the priority limiter. 0 = intreq[i] is not asserted and INT_SET bit is not set. 1 = intreq[i] is asserted or INT_SET bit is set.
30	W	0	INT_SET	Interrupt Set. Writes to this register have the following effect: 0 = No effect 1 = Makes INT_PENDING =1 and INT_PRIORITY is not updated. Reads to this register returns zero. Reset: INT_SET is inactive after reset.

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PRIORITY INTERRUPT CONTROLLER (T-PIC) REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
29	W	0	INT_CLR	Interrupt Clear. Writes to this register have the following effect: 0 = No effect 1 = Makes INT_PENDING = 0 if intreq[i] is not asserted and INT_PRIORITY is not updated. Reads to this register return zero. Reset: INT_CLR is inactive after reset.
28:8		-	Unused	Read as zero.
7:4	R	0	Reserved	May be used for future increase in the number of priority levels.
3:0	R/W	0	INT_PRIORITY	The INT_PRIORITY field determines the priority level of the intreq[i] line. This field is only written if INT_SET and INT_CLR are 0.

Offset 0x10 2018 *PIC_INT_REG_2*

Interrupt register 2. This register is identical to PIC_INT_REG_1 (0x10 2014).

Offset 0x10 201C *PIC_INT_REG_3*

Interrupt register 3. This register is identical to PIC_INT_REG_1 (0x10 2014).

Offset 0x10 2020 *PIC_INT_REG_4*

Interrupt register 4. This register is identical to PIC_INT_REG_1 (0x10 2014).

Offset 0x10 2024 *PIC_INT_REG_5*

USB Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).

Offset 0x10 2028 *PIC_INT_REG_6*

General Purpose IO Interrupt FIFO 0. This register is identical to PIC_INT_REG_1 (0x10 2014).

Offset 0x10 202C *PIC_INT_REG_7*

General Purpose IO Interrupt FIFO 1. This register is identical to PIC_INT_REG_1 (0x10 2014).

Offset 0x10 2030 *PIC_INT_REG_8*

General Purpose IO Interrupt FIFO 2. This register is identical to PIC_INT_REG_1 (0x10 2014).

Offset 0x10 2034 *PIC_INT_REG_9*

General Purpose IO Interrupt FIFO 3. This register is identical to PIC_INT_REG_1 (0x10 2014).

Offset 0x10 2038 *PIC_INT_REG_10*

General Purpose IO Interrupt TSU. This register is identical to PIC_INT_REG_1 (0x10 2014).

Offset 0x10 203C *PIC_INT_REG_11*

General Purpose IO TM-VIC Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).

Offset 0x10 2040 *PIC_INT_REG_12*

1394 FireWire™ Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).

Offset 0x10 2044 *PIC_INT_REG_13*

AICP 1 Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).

Offset 0x10 2048 *PIC_INT_REG_14*

AICP 2 Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).

Offset 0x10 204C *PIC_INT_REG_15*

I^2C 1 Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).

Offset 0x10 2050 *PIC_INT_REG_16*

I^2C 2 Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).

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PRIORITY INTERRUPT CONTROLLER (T-PIC) REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x10 2054			*PIC_INT_REG_17*	
Smartcard 1 Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 2058			*PIC_INT_REG_18*	
Smartcard 2 Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 205C			*PIC_INT_REG_19*	
UART 1 Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 2060			*PIC_INT_REG_20*	
UART 2 Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 2064			*PIC_INT_REG_21*	
UART 3 Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 2068			*PIC_INT_REG_22*	
PCI Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 206C			*PIC_INT_REG_23*	
T-PI bus controller error Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 2070			*PIC_INT_REG_24*	
M-PI bus controller error Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 2074			*PIC_INT_REG_25*	
F-PI bus controller error Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 2078			*PIC_INT_REG_26*	
2D Drawing Engine Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 207C			*PIC_INT_REG_27*	
MBS Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 2080			*PIC_INT_REG_28*	
MPEG Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 2084			*PIC_INT_REG_29*	
VIP 1 Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 2088			*PIC_INT_REG_30*	
VIP 2 Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 208C			*PIC_INT_REG_31*	
SPDIF Input Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 2090			*PIC_INT_REG_32*	
SPDIF Output Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 2094			*PIC_INT_REG_33*	
Audio Input 1 Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 2098			*PIC_INT_REG_34*	
Audio Output 1 Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 209C			*PIC_INT_REG_35*	
Audio Input 2 Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				

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PRIORITY INTERRUPT CONTROLLER (T-PIC) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 20A0			*PIC_INT_REG_36*	
Audio Output 2 Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 20A4			*PIC_INT_REG_37*	
Audio Input & Output 3 Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 20A8			*PIC_INT_REG_38*	
SSI Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 20AC			*PIC_INT_REG_39*	
MSP 1 MIPS Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 20B0			*PIC_INT_REG_40*	
MSP 1 TriMedia Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 20B4			*PIC_INT_REG_41*	
MSP 2 MIPS Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 20B8			*PIC_INT_REG_42*	
MSP 2 TriMedia Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 20BC			*PIC_INT_REG_43*	
Transport Stream DMA Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 20C0			*PIC_INT_REG_44*	
DMA Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 20C4			*PIC_INT_REG_45*	
ORCA 3D Drawing Engine Interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 20C8			*PIC_INT_REG_46*	
TriMedia debug interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 20CC			*PIC_INT_REG_47*	
PCI INTA interrupt. This register is identical to PIC_INT_REG_1 (0x03 E014).				
Offset 0x10 20D0			*PIC_INT_REG_48*	
Clocks module interrupt. This register is identical to PIC_INT_REG_1 (0x10 2014).				
Offset 0x10 20D4—2FF0			*Reserved*	
Offset 0x10 2FF4			*POWERDOWN*	
31	R/W	0	POWER_DOWN	Powerdown register for the module 0 = Normal operation of the peripheral. This is the reset value. 1 = Module is powered down and module clock can be removed. At powerdown, module responds to all reads with DEADABBA (except for reads of powerdown bit) and all writes with ERR ACK (except for writes to powerdown bit).
30:0		-	Unused	Ignore during writes and read as zeroes.
Offset 0x10 2FF8			*Reserved*	
Offset 0x10 2FFC			*PIC_MOD_ ID*	
31:16	R	0x011D	MODULE ID	The PIC module ID is 0x011D.

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PRIORITY INTERRUPT CONTROLLER (T-PIC) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
15:12	R	1	MAJREV	Major Revision
11:8	R	0	MINREV	Minor Revision
7:0	R	0	MODULE APERTURE SIZE	Aperture size = 4 kB*(bit_value+1)

TPBC Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.35)

T-PI BUS CONTROLLER (TPBC) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 3000			*TPBC_CTRL*	
31:5		-	Unused	Ignore upon read. Write as zeroes.
4:1	R/W	0x0	TOUT_SEL[3:0]	Timeout select 0x0 = Timeout generated after 1 wait cycle. 0x1 = Timeout generated after 3 consecutive wait cycles. 0x2 = Timeout generated after 7 consecutive wait cycles. 0x3 = Timeout generated after 15 consecutive wait cycles. 0x4 = Timeout generated after 31 consecutive wait cycles. 0x5 = Timeout generated after 63 consecutive wait cycles. 0x6 = Timeout generated after 127 consecutive wait cycles. 0x7 = Timeout generated after 255 consecutive wait cycles. 0x8 = Timeout generated after 511 consecutive wait cycles. 0x9 = Timeout generated after 1,023 consecutive wait cycles. 0xa = Timeout generated after 2,047 consecutive wait cycles. 0xb = Timeout generated after 4,095 consecutive wait cycles. 0xc = Timeout generated after 8,191 consecutive wait cycles. 0xd = Timeout generated after 16,383 consecutive wait cycles. 0xe = Timeout generated after 32,767 consecutive wait cycles. 0xf = Timeout generated after 65,535 consecutive wait cycles.
0	R/W	0x1	TOUT_OFF	Timeout disable 0x0 = Timeout enabled. 0x1 = Timeout disabled.
Offset 0x10 300C			*TPBC_ADDR*	
31:2	R	0x0000 0000-	ERR_TOUT_ADDR[31:2]	Full 30 bits of the T-PI address bus which causes a PI error or timeout.
1:0		-	Unused	Ignore upon read. Write as zeroes.
Offset 0x10 3010			*TPBC_STAT*	
31:30		-	Unused	Ignore upon read. Write as zeroes.

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T-PI BUS CONTROLLER (TPBC) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
29:16	R	0x00	ERR_TOUT_GNT[13:0]	Active master causing error or timeout 0x0001 = T-PI noise generator 0x0002 = GPIO 0x0004 = TS DMA 0x0008 = Audio Input 3 0x0010 = Audio Output 3 0x0020 = Audio Input 2 0x0040 = Audio Output 2 0x0080 = Audio Input 1 0x0100 = Audio Output 1 0x0200 = Sony Philips Digital Input 0x0400 = Sony Philips Digital Output 0x0800 = Synchronous Serial Interface 0x1000 = PI-PI cross over bridge 0x2000 = Trimedia
15		-	Unused	Ignore upon read. Write as zeroes.
14:10	R	0x00	ERR_TOUT_SEL[4:0]	Selected agent during error or timeout 0x00 = None 0x01 = PI-PI cross over bridge 0x02 = T-PI to Memory highway bus Interface (T-PIMI) 0x03 = Trimedia 0x04 = T-PI interrupt controller 0x05 = T-PI Bus controller 0x06 = GPIO 0x07 = Video MPEG2 0x08 = Video Input Processor 1 0x09 = Video Input Processor 2 0x0a = Synchronous Serial Interface 0x0b = Sony Philips Digital Output 0x0c = Sony Philips Digital Input 0x0d = Memory Based Scalar 0x0e = Image Composition Processor 1 0x0f = Image Composition Processor 2
	R	0x00	ERR_TOUT_SEL[4:0]	Selected agent during error or timeout (cont'd.) 0x10 = Audio Output 1 0x11 = Audio Input 1 0x12 = Audio Output 2 0x13 = Audio Input 2 0x14 = Audio Output 3 0x15 = Audio Input 3 0x16 = MPEG System Processor 1 0x17 = MPEG System Processor 2 0x18 = MPEG System Processor 3 0x19 = TSDMA 0x1a = Null 1 0x1b = Null 2 0x1c = Null 3 0x1d = Null 4 0x1e = Default slave
9		-	Unused	Ignore upon read. Write as zeroes.
8:4	R	0x00	ERR_OPC[4:0]	Opcode causing error or timeout. See bits 12:8 of the FPBC_STAT register (offset 0x03_F010) for the Opcode table.
3		-	Unused	Ignore upon read. Write as zeroes.
2:0	R	0x00	ERR_ACK[2:0]	Acknowledge during error or timeout. See bits 2:0 of the FPBC_STAT register (offset 0x03_F010) for the ACKs table.

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T-PI BUS CONTROLLER (TPBC) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 3014			*TPBC_MON*	
31:30		-	Unused	Ignore upon read. Write as zeroes.
29:16	R	0x000	GNT_LAST[13:0]	Last active master 0x0001 = T-PI noise generator 0x0002 = GPIO 0x0004 = TS DMA 0x0008 = Audio Input 3 0x0010 = Audio Output 3 0x0020 = Audio Input 2 0x0040 = Audio Output 2 0x0080 = Audio Input 1 0x0100 = Audio Output 1 0x0200 = Sony Philips Digital Input 0x0400 = Sony Philips Digital Output 0x0800 = Synchronous Serial Interface 0x1000 = PI-PI cross over bridge 0x2000 = TriMedia
15:14		-	Unused	Ignore upon read. Write as zeroes.
13:0	R	0x000	REQ_CURR[13:0]	Current requests 0x0001 = T-PI noise generator 0x0002 = GPIO 0x0004 = TS DMA 0x0008 = Audio Input 3 0x0010 = Audio Output 3 0x0020 = Audio Input 2 0x0040 = Audio Output 2 0x0080 = Audio Input 1 0x0100 = Audio Output 1 0x0200 = Sony Philips Digital Output 0x0400 = Sony Philips Digital Input 0x0800 = Synchronous Serial Interface 0x1000 = PI-PI cross over bridge 0x2000 = TriMedia
Offset 0x10 3FE0			*TPBC_INT_STATUS*	
31:2		-	Unused	Ignore upon read. Write as zeroes.
1	R	0	INT_STATUS_TOUT	Timeout interrupt status. Reports any pending timeout interrupts: 0x1 = Timeout interrupt pending: T-PI bus controller has generated a timeout because a T-PI device has violated the programmable limit for timeout (see TPBC_TOUT). Or M-bridge or C-bridge generated a timeout request (see PI-PI bridge). 0x0 = Timeout interrupt is not pending.
0	R	0	INT_STATUS_ERROR	Error interrupt status. Reports any pending error interrupts: 0x1 = Error interrupt pending, meaning F-PI bus controller has detected an error acknowledge on the M-PI bus. 0x0 = Error interrupt is not pending.
Offset 0x10 3FE4			*TPBC_INT_EN*	
31:2		-	Unused	Ignore upon read. Write as zeroes.
1	R/W	0	INT_ENABLE_TOUT	Timeout interrupt enable register 0x1 = Timeout interrupt is enabled 0x0 = Timeout interrupt is disabled.
0	R/W	0	INT_ENABLE_ERROR	Timeout interrupt enable register 0x1 = Error interrupt is enabled 0x0 = Error interrupt is disabled.

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T-PI BUS CONTROLLER (TPBC) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 3FE8			*TPBC_INT_CLR*	
31:2		-	Unused	Ignore upon read. Write as zeroes.
1	W	0	INT_CLEAR_TOUT	Timeout interrupt clear register. This is written by software to clear the interrupt. 0x1 = Timeout interrupt is cleared 0x0 = Timeout interrupt is not cleared.
0	W	0	INT_CLEAR_ERROR	Error interrupt clear register. This is written by software to clear the interrupt. 0x1 = Error interrupt is cleared 0x0 = Error interrupt is not cleared.
Offset 0x10 3FEC			*TPBC_INT_SET*	
31:2		-	Unused	Ignore upon read. Write as zeroes.
1	W	0	INT_SET_TOUT	Timeout interrupt set register. Allows software to set interrupts. 0x1 = Timeout interrupt is set 0x0 = Timeout interrupt is not set.
0	W	0	INT_SET_ERROR	Error interrupt set register. Allows software to set interrupts. 0x1 = Error interrupt is set 0x0 = Error interrupt is not set.
Offset 0x10 3FFC			*TPBC_MODULE_ID*	
31:16	R	0x0112	MODULE_ID[15:0]	Unique 16-bit code. Module ID 0 and 1 are reserved for future use. Value 0x0112 is for the PNX8525 T-PI Bus controller module.
15:12	R	1	MAJREV[3:0]	Major Revision: any revision that might break software compatibility.
11:8	R	0	MINREV[3:0]	Minor Revision: any revision that maintains software compatibility.
7:0	R	0	MODULE_APERTURE_SIZE[7:0]	Aperture size = 4 kB*(bit_value+1), so 0 means 4 kB (the default).

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GPIO Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.10)

GPIO REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
GPIO Mode Control				
Offset 0x10 4000			*Mode Control for GPIOs 15—0*	
31:30	R/W	0b11	MC for GPIO number 15	The Mode Control (MC) bit pairs control the mode of the corresponding GPIO pin. The number portion of MCxx identifies the GPIO number. Refer to *PNX8526 User Manual, Ref. UM10104_1, Chap.10)* The following values apply to writing to all of the bit pairs: 00 = Retain current GPIO Mode of operation (will not overwrite current mode). Not readable 01 = Place pin in primary function mode (see MUX table). 10 = Place pin in GPIO function mode (see MUX table). 11 = Place pin in GPIO function with open-drain output mode.
29:28	R/W	0b11	MC for GPIO number 14	
27:26	R/W	0b11	MC for GPIO number 13	
25:24	R/W	0b11	MC for GPIO number 12	
23:22	R/W	0b11	MC for GPIO number 11	
21:20	R/W	0b11	MC for GPIO number 10	
19:18	R/W	0b11	MC for GPIO number 09	
17:16	R/W	0b11	MC for GPIO number 08	
15:14	R/W	0b11	MC for GPIO number 07	
13:12	R/W	0b11	MC for GPIO number 06	
11:10	R/W	0b11	MC for GPIO number 05	
9:8	R/W	0b11	MC for GPIO number 04	
7:6	R/W	0b11	MC for GPIO number 03	
5:4	R/W	0b11	MC for GPIO number 02	
3:2	R/W	0b11	MC for GPIO number 01	
1:0	R/W	0b11	MC for GPIO number 00	
Offset 0x10 4004			*Mode Control for GPIOs 31—16*	
31:30	R/W	0b11	MC for GPIO number 31	The Mode Control (MC) bit pairs control the mode of the corresponding GPIO pin. The number portion of MCxx identifies the GPIO number. Refer to *PNX8526 User Manual, Ref. UM10104_1, Chap.10)* The following values apply to writing to all of the bit pairs: 00 = Retain current GPIO Mode of operation (will not overwrite current mode). Not readable 01 = Place pin in primary function mode (see MUX table). 10 = Place pin in GPIO function mode (see MUX table). 11 = Place pin in GPIO function with open-drain output mode.
29:28	R/W	0b11	MC for GPIO number 30	
27:26	R/W	0b11	MC for GPIO number 29	
25:24	R/W	0b11	MC for GPIO number 28	
23:22	R/W	0b11	MC for GPIO number 27	
21:20	R/W	0b11	MC for GPIO number 26	
19:18	R/W	0b11	MC for GPIO number 25	
17:16	R/W	0b11	MC for GPIO number 24	
15:14	R/W	0b11	MC for GPIO number 23	
13:12	R/W	0b11	MC for GPIO number 22	
11:10	R/W	0b11	MC for GPIO number 21	
9:8	R/W	0b11	MC for GPIO number 20	
7:6	R/W	0b11	MC for GPIO number 19	
5:4	R/W	0b11	MC for GPIO number 18	
3:2	R/W	0b11	MC for GPIO number 17	
1:0	R/W	0b11	MC for GPIO number 16	

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GPIO REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 4008			*Mode Control for GPIOs 47—32*	
31:30	R/W	0b11	MC for GPIO number 47	The Mode Control (MC) bit pairs control the mode of the corresponding GPIO pin. The number portion of MCxx identifies the GPIO number. Refer to *PNX8526 User Manual, Ref. UM10104_1, Chap.10)* The following values apply to writing to all of the bit pairs: 00 = Retain current GPIO Mode of operation (will not overwrite current mode). Not readable 01 = Place pin in primary function mode (see MUX table). 10 = Place pin in GPIO function mode (see MUX table). 11 = Place pin in GPIO function with open-drain output mode.
29:28	R/W	0b11	MC for GPIO number 46	
27:26	R/W	0b11	MC for GPIO number 45	
25:24	R/W	0b11	MC for GPIO number 44	
23:22	R/W	0b11	MC for GPIO number 43	
21:20	R/W	0b11	MC for GPIO number 42	
19:18	R/W	0b11	MC for GPIO number 41	
17:16	R/W	0b11	MC for GPIO number 40	
15:14	R/W	0b11	MC for GPIO number 39	
13:12	R/W	0b11	MC for GPIO number 38	
11:10	R/W	0b11	MC for GPIO number 37	
9:8	R/W	0b11	MC for GPIO number 36	
7:6	R/W	0b11	MC for GPIO number 35	
5:4	R/W	0b11	MC for GPIO number 34	
3:2	R/W	0b11	MC for GPIO number 33	
1:0	R/W	0b11	MC for GPIO number 32	
Offset 0x10 400C			*Mode Control for GPIOs 60—48*	
31:26		-	Unused	
25:24	R/W	0b11	MC for GPIO number 60	The Mode Control (MC) bit pairs control the mode of the corresponding GPIO pin. The number portion of MCxx identifies the GPIO number. Refer to *PNX8526 User Manual, Ref. UM10104_1, Chap.10)* The following values apply to writing to all of the bit pairs: 00 = Retain current GPIO Mode of operation (will not overwrite current mode). Not readable 01 = Place pin in primary function mode (see MUX table). 10 = Place pin in GPIO function mode (see MUX table). 11 = Place pin in GPIO function with open-drain output mode.
23:22	R/W	0b11	MC for GPIO number 59	
21:20	R/W	0b11	MC for GPIO number 58	
19:18	R/W	0b11	MC for GPIO number 57	
17:16	R/W	0b11	MC for GPIO number 56	
15:14	R/W	0b11	MC for GPIO number 55	
13:12	R/W	0b11	MC for GPIO number 54	
11:10	R/W	0b11	MC for GPIO number 53	
9:8	R/W	0b11	MC for GPIO number 52	
7:6	R/W	0b11	MC for GPIO number 51	
5:4	R/W	0b11	MC for GPIO number 50	
3:2	R/W	0b11	MC for GPIO number 49	
1:0	R/W	0b11	MC for GPIO number 48	

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GPIO REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
GPIO Data Control				
Offset 0x10 4010			*Mask and IO Data for GPIOs 15—0*	
31:16	R/W	0x0000	MASK[15:00]	Mask IOD 0 0 Retains current stored data (will not overwrite current data). Not readable. 0 1 Sets the corresponding GPIO pin in tri-state mode, allowing the pin to be used as data input. 1 0 GPIO output mode. Drives a generated pattern (if enabled) or IOD (‘0’ in this case) onto the corresponding GPIO pin. 1 1 GPIO output mode. Drives a generated pattern (if enabled) or IOD (‘1’ in this case) onto the corresponding GPIO pin. Note: If open-drain mode is selected, drive to ‘1’ is disabled.
15:0	R/W	0xFFFF	IOD[15:00]	
Offset 0x10 4014			*Mask and IO Data for GPIOs 31—16*	
31:16	R/W	0x0000	MASK[31:16]	See Mask and IO data for GPIOs 15-0 (0x10 4010) for bit descriptions.
15:0	R/W	0xFFFF	IOD[31:16]	
Offset 0x10 4018			*Mask and IO Data for GPIOs 47—32*	
31:16	R/W	0x0000	MASK[47:32]	See Mask and IO data for GPIOs 15-0 (0x10 4010) for bit descriptions.
15:0	R/W	0xFFFF	IOD[47:32]	
Offset 0x10 401C			*Mask and IO Data for GPIOs 60—48*	
31:29		-	Unused	See Mask and IO data for GPIOs 15-0 (0x10 4010) for bit descriptions.
28:16	R/W	0x0000	MASK[60:48]	
15:13		-	Unused	See Mask and IO data for GPIOs 15-0 (0x10 4010) for bit descriptions.
12:0	R/W	0xFFFF	IOD[60:48]	

GPIO REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Readable Internal PNX8525 Signals				
Offset 0x10 4020			*Internal Signals*	
31:15		-	Unused]	
19	R	0	last_word_q3	Reads value of GPIOs last 32-bit word timestamp for Queue 3.
18	R	0	last_word_q2	Reads value of GPIOs last 32-bit word timestamp for Queue 2.
17	R	0	last_word_q1	Reads value of GPIOs last 32-bit word timestamp for Queue 1.
16	R	0	last_word_q0	Reads value of GPIOs last 32-bit word timestamp for Queue 0.
15	R	0	tsdma_tstamp2	Reads value of TSDMA timestamp 2 signal input to the GPIO module.
14	R	0	tsdma_tstamp1	Reads value of TSDMA timestamp 1 signal input to the GPIO module.
13	R	0	vip2_eow_aux	Reads value of VIP2 end of aux window timestamp signal input to the GPIO module.

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GPIO REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
12	R	0	vip2_eow_vid	Reads value of VIP2 end of vid window timestamp signal input to the GPIO module.
11	R	0	vip1_eow_aux	Reads value of VIP 1 end of aux window timestamp signal input to the GPIO module.
10	R	0	vip1_eow_vid	Reads value of VIP 1 end of vid window timestamp signal input to the GPIO module.
9	R	0	icp2_tstamp	Reads value of ICP 2 timestamp signal input to the GPIO module.
8	R	0	icp1_tstamp	Reads value of ICP 1 timestamp signal input to the GPIO module.
7	R	0	spdi_tstamp2	Reads value of SPDIF IN timestamp 2 signal input to the GPIO module.
6	R	0	spdi_tstamp1	Reads value of SPDIF IN timestamp 1 (word select timestamp) signal input to the GPIO module.
5	R	0	spdo_tstamp	Reads value of SPDIF OUT timestamp signal input to the GPIO module.
4	R	0	ai2_tstamp	Reads value of Audio IN 2 timestamp signal input to the GPIO module.
3	R	0	ai1_tstamp	Reads value of Audio IN 1 timestamp signal input to the GPIO module.
2	R	0	ao2_tstamp	Reads value of Audio OUT 2 timestamp signal input to GPIO module.
1	R	0	ao1_tstamp	Reads value of Audio OUT 1 timestamp signal input to GPIO module.
0	R	0	aio_tstamp	Reads value of Audio IO IN timestamp signal input to the GPIO module.

GPIO REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x10 4024			*GPIO_EV0*	
31		-	Unused	
30	R/W	0	EN_EV_TSTAMP	Enables an event timestamp signal to be generated whenever the last 32-bit word from a DMA buffer reaches the GPIO output pins. This field is only valid in Pattern Generating modes (FIFO_MODE[1]=1).
29	R/W	0	EN_IR_CARRIER	Enables a subcarrier IR transmission. FREQ_DIV[15:0] is combined with CARRIER_DIV[4:0] to generated sub-carrier and TX frequencies. 0 = IR Carrier disabled, CARRIER_DIV[4:0] not used. 1 = IR Carrier enabled, CARRIER_DIV[4:0] used. Note: This field is only valid in Pattern Generation using sample mode (FIFO_MODE=11) with EN_CLOCK_SEL disabled.
28	R/W	0	EN_IR_FILTER	Enables a received IR signal to be filtered. No signal pulses less than the period programmed in IR_FILTER are passed through to the monitoring logic. Note: This field is only valid in Signal Sampling mode (FIFO_MODE=01) with EN_CLOCK_SEL disabled.

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GPIO REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
27:26	R/W	0	EN_CLOCK_SEL	In Signal Sampling mode, this bit enables an input signal selected by CLOCK_SEL to be used to sample the input signal selected by IO_SEL. 00,10 = CLOCK_SEL disabled. 01 = CLOCK_SEL enabled, sample on positive edge. 11 = CLOCK_SEL enabled, sample on negative edge. In Pattern Generation using sample mode, this bit enables an output signal selected by CLOCK_SEL to be used to output the sampling frequency. This feature is valid if sampling frequency is less than 108 MHz. 00,10 = CLOCK_SEL disabled. 01 = CLOCK_SEL enabled, output clk at sampling freq. 11 = CLOCK_SEL enabled, output inverted clk at sampling freq. Note: This field is only valid in Signal Sampling mode (FIFO_MODE=01) and Pattern Generation using sample mode (FIFO_MODE=11).
25:18	R/W	0	CLOCK_SEL	In Signal Sampling mode, this field selects the GPIO input pin to be used to 'sample' the signal(s) selected by IO_SEL. Note: The GPIO input used for sampling must be slower than 108 MHz. In Pattern Generation using sample mode, this field selects which GPIO output pin to output the sampling frequency clock on. Note: This field is only valid in Signal Sampling mode (FIFO_MODE=01) and Pattern Generation using sample mode (FIFO_MODE=11). Refer to *PNX8526 User Manual, Ref. UM10104_1, Chap.10)* for field values.
17:16	R/W	0	EN_IO_SEL	This field selects how many GPIO pins should be sampled in one FIFO queue: 00,11 = IO_SEL_0 enabled: 1-bit samples. 01 = IO_SEL_0 and IO_SEL_1 enabled: 2-bit samples. 10 = IO_SEL_0, IO_SEL_1, IO_SEL_2 and IO_SEL_3 enabled: 4-bit samples. Note: This field is only valid in Signal Sampling mode (FIFO_MODE=01) or Pattern Generation using sample mode (FIFO_MODE=11). In all other modes only IO_SEL_0 is enabled.
15:4	R/W	0	INTERVAL	Interval of silence. If a change is monitored on a signal and no more signal activity is monitored for a time equal to the interval of silence, writing to the current buffer is halted and a BUFx_RDY interrupt is generated. Writing continues to the alternate buffer. This field is only valid if FIFO_MODE[1:0] = 00. 0x000 = Disabled. 0x001 = 1x128 13.5 MHz period, 9.48 µs 0x002 = 2x128 13.5 MHZ periods, 18.96 µs 0x003 = 3x128 13.5 MHZ periods, 28,44 µs .... 0x3FFh = 1023x128 13.5 MHz period, 9.69 ms .... 0xFFF = 4095x128 13.5 MHz period, 38.8 ms Note: Field in only valid in Event Timestamping mode (FIFO_MODE=00, EVENT_MODE>00).
3:2	R/W	0	EVENT_MODE	Timestamping event mode: 00 = Event detection disabled. 01 = Capture negative edge. 10 = Capture positive edge. 11 = Capture either edge. Note: Field is valid in Event Timestamping mode(FIFO_MODE[1:0]=00).

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GPIO REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
1:0	R/W	0	FIFO_MODE	This bit selects what mode of operation the FIFO queue is in: 00 = Event Timestamping (or Disabled if EVENT_MODE[1:0] = 00) 01 = Signal Sampling 10 = Pattern Generation using timestamps. 11 = Pattern Generation using samples.
Offset 0x10 4028			*GPIO_EV1*	
Refer to GPIO_EV0 at offset 0x10 4024 for descriptions.				
Offset 0x10 402C			*GPIO_EV2*	
Refer to GPIO_EV0 at offset 0x10 4024 for descriptions.				
Offset 0x10 4030			*GPIO_EV3*	
Refer to GPIO_EV0 at offset 0x10 4024 for descriptions.				
Signal Monitoring Control Registers for the Timestamp Units				
Offset 0x10 4034			*GPIO_EV4*	
31:10		-	Unused	
9:2	R/W	0	IO_SEL	This field selects the GPIO pin or internal global signal to be monitored. Refer to *PNX8526 User Manual, Ref. UM10104_1, Chap.10)* for field values. Note: IO_SEL cannot be written to unless timestamping is disabled (EVENT_MODE=00).
1:0	R/W	0	EVENT_MODE	Timestamping event mode: 00 = Event detection disabled. 01 = Capture negative edge. 10 = Capture positive edge. 11 = Capture either edge.
Offset 0x10 4038			*GPIO_EV5*	
Refer to GPIO_EV4 at offset 0x10 4034 for descriptions.				
Offset 0x10 403C			*GPIO_EV6*	
Refer to GPIO_EV4 at offset 0x10 4034 for descriptions.				
Offset 0x10 4040			*GPIO_EV7*	
Refer to GPIO_EV4 at offset 0x10 4034 for descriptions.				
Offset 0x10 4044			*GPIO_EV8*	
Refer to GPIO_EV4 at offset 0x10 4034 for descriptions.				
Offset 0x10 4048			*GPIO_EV9*	
Refer to GPIO_EV4 at offset 0x10 4034 for descriptions.				
Offset 0x10 404C			*GPIO_EV10*	
Refer to GPIO_EV4 at offset 0x10 4034 for descriptions.				
Offset 0x10 4050			*GPIO_EV11*	
Refer to GPIO_EV4 at offset 0x10 4034 for descriptions.				
Offset 0x10 4054			*GPIO_EV12*	
Refer to GPIO_EV4 at offset 0x10 4034 for descriptions.				

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GPIO REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 4058			*GPIO_EV13*	
Refer to GPIO_EV4 at offset 0x10 4034 for descriptions.				
Offset 0x10 405C			*GPIO_EV14*	
Refer to GPIO_EV4 at offset 0x10 4034 for descriptions.				
Offset 0x10 4060			*GPIO_EV15*	
Refer to GPIO_EV4 at offset 0x10 4034 for descriptions.				

GPIO REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Monitoring and Pattern Generation Control Registers				
Offset 0x10 4064			*IO_SEL0*	
Note: IO_SEL cannot be written to unless all signal generation and monitoring is disabled (FIFO_MODE=00;EVENT_MODE=00).				
31:24	R/W	0	IO_SEL_3	This field selects a GPIO pin which should be merged with the GPIO pin selected by IO_SEL_0, IO_SEL_1 and IO_SEL_2 to enable 4-bit samples in one FIFO queue. This field is only used in Signal Sampling mode and Pattern Generation using sample mode and is enabled by EN_IO_SEL
23:16	R/W	0	IO_SEL_2	This field selects a GPIO pin which should be merged with the GPIO pins selected by IO_SEL_0, IO_SEL_1 and IO_SEL_3 to enable 4-bit samples in one FIFO queue. This field is only used in Signal Sampling mode and Pattern Generation using sample mode and is enabled by EN_IO_SEL
15:8	R/W	0	IO_SEL_1	This field selects a GPIO pin which should be merged with the GPIO pin selected by IO_SEL_0 to enable 2-bit samples in one FIFO queue. This field is only used in Signal Sampling mode and Pattern Generation using sample mode and is enabled by EN_IO_SEL
7:0	R/W	0	IO_SEL_0	In Signal Monitoring modes (FIFO_MODE[1]=0) this field selects the GPIO pin or internal global signal to be observed. In Pattern Generation modes (FIFO_MODE[1]=1) this field selects the GPIO pin which is to be driven. Refer to *PNX8526 User Manual, Ref. UM10104_1, Chap.10)* for field values.
Offset 0x10 4068			*IO_SEL1*	
Refer to IO_SEL0 at offset 0x10 4064 for descriptions.				
Offset 0x10 406C			*IO_SEL2*	
Refer to IO_SEL0 at offset 0x10 4064 for descriptions.				
Offset 0x10 4070			*IO_SEL3*	
Refer to IO_SEL0 at offset 0x10 4064 for descriptions.				
Offset 0x10 4074			*PG_BUF_CTRL0*	
31:18		-	Unused	

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GPIO REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
17:0	R/W	0	BUF_LEN	This field indicates how many valid 32-bit words software has written to a DMA buffer. When BUF1_RDY is cleared, the BUF_LEN value is loaded for DMA buffer 1. When BUF2_RDY is cleared, the BUF_LEN value is loaded for DMA buffer 2. The 18-bit field allows DMA buffer lengths as large as 1 MB. 0x00000 = One 32-bit word 0x00001 = Two 32-bit words 0x3FFFF = 262143 32-bit words Note: This field is valid in Pattern Generation modes (FIFO_MODE [1] = 1).
Offset 0x10 4078			*PG_BUF_CTRL1*	
Refer to PG_BUF_CTRL0 at offset 0x10 4074 for descriptions.				
Offset 0x10 407C			*PG_BUF_CTRL2*	
Refer to PG_BUF_CTRL0 at offset 0x10 4074 for descriptions.				
Offset 0x10 4080			*PG_BUF_CTRL3*	
Refer to PG_BUF_CTRL0 at offset 0x10 4074 for descriptions.				
Offset 0x10 4084			*BASE1_PTR0*	
31:2	R/W	0	BASE1_PTR	Start byte address for DMA buffer 1 of FIFO queue.
1:0		-	Unused	
Offset 0x10 4088			*BASE1_PTR1*	
Refer to BASE1_PTR0 at offset 0x10 4084 for descriptions.				
Offset 0x10 408C			*BASE1_PTR2*	
Refer to BASE1_PTR0 at offset 0x10 4084 for descriptions.				
Offset 0x10 4090			*BASE1_PTR3*	
Refer to BASE1_PTR0 at offset 0x10 4084 for descriptions.				
Offset 0x10 4094			*BASE2_PTR0*	
31:2	R/W	0	BASE2_PTR	Start byte address for DMA buffer 2 of FIFO queue.
1:0		-	Unused	
Offset 0x10 4098			*BASE2_PTR1*	
Refer to BASE2_PTR0 at offset 0x10 4094 for descriptions.				
Offset 0x10 409C			*BASE2_PTR2*	
Refer to BASE2_PTR0 at offset 0x10 4094 for descriptions.				
Offset 0x10 40A0			*BASE2_PTR3*	
Refer to BASE2_PTR0 at offset 0x10 4094 for descriptions.				
Offset 0x10 40A4			*SIZE0*	
31:20		-	Unused	
13:0	R/W	0	SIZE	Size, in 64-byte multiples, of each of the two DMA buffers. 0x0001 = 64 bytes 0x0002 = 128 bytes .... 0x3FFF = 1 MB
Offset 0x10 40A8			*SIZE1*	
Refer to SIZE0 at offset 0x10 40A4 for descriptions.				

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GPIO REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 40AC			*SIZE2*	
Refer to SIZE0 at offset 0x10 40A4 for descriptions.				
Offset 0x10 40B0			*SIZE3*	
Refer to SIZE0 at offset 0x10 40A4 for descriptions.				
Offset 0x10 40B4			*DIVIDER0*	
31:23		-	Unused	
22:21	R/W	0	DUTY_CYCLE	This field selects the duty cycle for subcarriers. 00 = 33% duty-cycle 01 = 50% duty-cycle 10 = 66% duty cycle 11 = Illegal This field is only valid in pattern generation modes and when EN_IR_CARRIER=1.
20:16	R/W	00	CARRIER_DIV (when FIFO_MODE[1] =1)	Used in IR TX applications if a subcarrier is required for transmission. To enable this divider EN_IR_CARRIER=1. If enabled, the IR subcarrier frequency is defined by programming FREQ_DIV. The 'ONTIME' is defined by FREQ_DIV x CARRIER_DIV. 0x00, 0x01 = Disabled. 0x02 = Sampling frequency is FREQ_DIV/2. ..... 0x1F = Sampling frequency is FREQ_DIV/31.
18:16		00	IR_FILTER (when FIFO_MODE[1] =0)	Used in IR RX applications to filter a received IR signal. To enable this divider EN_IR_FILTER=1. If enabled, IR pulses greater than IR_FILTER are passed through to the signal monitoring logic. 0x0 = 54/108 MHz, 0.5 µs 0x1 = 108/108 MHz, 1 µs 0x2 = 162/108 MHz, 1.5 µs 0x3 = 216/108 MHz, 2 µs 0x4 = 270/108 MHz, 2.5 µs 0x5 = 324/108 MHz, 3 µs 0x6 = 378/108 MHz, 3.5 µs 0x7 = 432/108 MHz, 4 µs Note: The filter operates on one input per queue. This bit is the input selected by IO_SEL[7:0]. If used in multi-bit sampling modes (IO_SEL_EN = 01/10) be aware that the filtered signal is delayed by the selected IR_FILTER value with respect to the other signals sampled in the queue.
15:0	R/W	0000	FREQ_DIV	16-bit Frequency Divider for signal sampling and pattern generation using samples. If EN_CARRIER_FREQ = 0 Sampling Freq. = 108 MHz/FREQ_DIV 0x0000 = Disabled. 0x0001 = Sampling frequency is 108 MHz 0x0002 = Sampling/Carrier frequency is 54 MHz ..... 0xFFFF = Sampling/Carrier frequency is 1.648 kHz If EN_CARRIER_FREQ = 1 Carrier Freq. = 54 MHz/FREQ_DIV 0x0000 = Disabled. 0x0001 = Carrier frequency is 54 MHz 0x0002 = Carrier frequency is 26 MHz ..... 0xFFFF = Carrier frequency is 824 Hz

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GPIO REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x10 40B8			*DIVIDER1*	
Refer to DIVIDER0 at offset 0x10 40B4 for descriptions.				
Offset 0x10 40BC			*DIVIDER2*	
Refer to DIVIDER0 at offset 0x10 40B4 for descriptions.				
Offset 0x10 40C0			*DIVIDER3*	
Refer to DIVIDER0 at offset 0x10 40B4 for descriptions.				

GPIO REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Timestamp Unit Registers				
Offset 0x10 40C4			*TSU0*	
31	R	0	Direction	This field indicates the direction of the event which occurred: 0 = A falling edge 1 = A rising edge
30:0	R	0	Timestamp	This field holds the 31-bit timestamp.
Offset 0x10 40C8			*TSU1*	
Refer to TSU0 at offset 0x10 40C4 for descriptions.				
Offset 0x10 40CC			*TSU2*	
Refer to TSU0 at offset 0x10 40C4 for descriptions.				
Offset 0x10 40D0			*TSU3*	
Refer to TSU0 at offset 0x10 40C4 for descriptions.				
Offset 0x10 40D4			*TSU4*	
Refer to TSU0 at offset 0x10 40C4 for descriptions.				
Offset 0x10 40D8			*TSU5*	
Refer to TSU0 at offset 0x10 40C4 for descriptions.				
Offset 0x10 40DC			*TSU6*	
Refer to TSU0 at offset 0x10 40C4 for descriptions.				
Offset 0x10 40E0			*TSU7*	
Refer to TSU0 at offset 0x10 40C4 for descriptions.				
Offset 0x10 40E4			*TSU8*	
Refer to TSU0 at offset 0x10 40C4 for descriptions.				
Offset 0x10 40E8			*TSU9*	
Refer to TSU0 at offset 0x10 40C4 for descriptions.				
Offset 0x10 40EC			*TSU10*	
Refer to TSU0 at offset 0x10 40C4 for descriptions.				
Offset 0x10 40F0			*TSU11*	
Refer to TSU0 at offset 0x10 40C4 for descriptions.				

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GPIO REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
GPIO Time Counter				
Offset 0x10 40F4			*TIME_CTR*	
31		-	Unused	
30:0	R	0	TIME_CTR	GPIO master time counter. It is incremented at a frequency of 13.5 MHz.
GPIO TM Timer Input Select				
Offset 0x10 40F8			*TIMER_IO_SEL*	
31:16		-	Unused	
15:8	R/W	0	TIMER_IO_SEL1	Selects GPIO or internal input to be output onto gpio_timer[1]. See *PNX8526 User Manual, Ref. UM10104_1, Chap.10)* for valid values.
7:0	R/w	0	TIMER_IO_SEL0	Selects GPIO or internal input to be output onto gpio_timer[0]. See *PNX8526 User Manual, Ref. UM10104_1, Chap.10)* for valid values.
VIC Interrupt Status				
Offset 0x10 40FC			*VIC_INT_STATUS*	
31:5		-	Unused	
4	R	0	TSU Status	TSU status bit for interrupts of the 12 TSUs (ORed together)
3	R	0	FIFO Queue 3 status	FIFO Queue 3 status bit for all interrupts (ORed together)
2	R	0	FIFO Queue 2 status	FIFO Queue 2 status bit for all interrupts (ORed together)
1	R	0	FIFO Queue 1 status	FIFO Queue 1 status bit for all interrupts (ORed together)
0	R	0	FIFO Queue 0 status	FIFO Queue 0 status bit for all interrupts (ORed together)
Offset 0x10 4100—4F9C			*Reserved*	

GPIO REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
GPIO Interrupt Registers for the FIFO Queues				
Offset 0x10 4FA0			*INT_STATUS0*	
31:14	R	0	VALID_PTR	Indicates how many valid 32-bit words of data have been written by the GPIO to the current DMA buffer. 0x00000 = One 32-bit word 0x00001 = Two 32-bit words ..... 0x3FFFF = 262143 32-bit words When a BUFx_RDY signal occurs, the address to read from can be calculated using VALID_PTR. This field is only updated by the GPIO after the relevant BUFx_RDY flag is cleared by software. It is valid in SIgnal Monitoring modes only.
5:4	R	0	Reserved	
3	R	0	INT_OE	Internal overrun error. Internal GPIO data buffer has overrun before data has been written to external DMA buffer. Data has been lost. ONLY USED in signal monitoring modes.

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GPIO REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
2	R	0	FIFO_OE	FIFO overrun error. A new, empty DMA buffer was not supplied in time. ONLY USED in signal monitoring modes.
1	R	0	BUF2_RDY	In Signal Monitoring mode: DMA buffer 2 is ready to be read. It is either full or an interval of silence has occurred. In Pattern Generation mode: Contents of DMA buffer 2 have been read.
0	R	0	BUF1_RDY	In Signal Monitoring mode: DMA buffer1 is ready to be read. It is either full or an interval of silence has occurred. In Pattern Generation mode: Contents of DMA buffer 1 have been read.
Offset 0x10 4FA4			*INT_ENABLE0*	
31:4		-	Unused	
3	R/W	0	INT_OE_EN	Active high Internal overrun error interrupt enable for queue 0
2	R/W	0	FIFO_OE_EN	Active high FIFO overrun error interrupt enable for queue 0
1	R/W	0	BUF2_RDY_EN	Active high Buffer 2 ready interrupt enable for queue 0
0	R/W	0	BUF1_RDY_EN	Active high Buffer 1 ready interrupt enable for queue 0
Offset 0x10 4FA8			*INT_CLEAR0*	
31:4		-	Unused	
3	W	0	INT_OE_CLR	Active high internal overrun error interrupt clear for queue 0
2	W	0	FIFO_OE_CLR	Active high FIFO overrun error interrupt clear for queue 0
1	W	0	BUF2_RDY_CLR	Active high Buffer 2 ready interrupt clear for queue 0
0	W	0	BUF1_RDY_CLR	Active high Buffer 1 ready interrupt clear for queue 0
Offset 0x10 4FAC			*INT_SET0*	
31:4		-	Unused	
3	W	0	INT_OE_SET	Active high internal overrun error interrupt set for queue 0
2	W	0	FIFO_OE_SET	Active high FIFO overrun error interrupt set for queue 0
1	W	0	BUF2_RDY_SET	Active high Buffer 2 ready interrupt set for queue 0
0	W	0	BUF1_RDY_SET	Active high Buffer 1 ready interrupt set for queue 0
Offset 0x10 4FB0			*INT_STATUS1*	
Refer to INT_STATUS0 at offset 0x10 4FA0 for descriptions.				
Offset 0x10 4FB4			*INT_ENABLE1*	
Refer to INT_ENABLED0 at offset 0x10 4FA4 for descriptions.				
Offset 0x10 4FB8			*INT_CLEAR1*	
Refer to INT_CLEAR0 at offset 0x10 4FA8 for descriptions.				
Offset 0x10 4FBC			*INT_SET1*	
Refer to INT_SET0 at offset 0x10 4FAC for descriptions.				
Offset 0x10 4FC0			*INT_STATUS2*	
Refer to INT_STATUS0 at offset 0x10 4FA0 for descriptions.				
Offset 0x10 4FC4			*INT_ENABLE2*	
Refer to INT_ENABLED0 at offset 0x10 4FA4 for descriptions.				

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GPIO REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x10 4FC8			*INT_CLEAR2*	
Refer to INT_CLEAR0 at offset 0x10 4FA8 for descriptions.				
Offset 0x10 4FCC			*INT_SET2*	
Refer to INT_SET0 at offset 0x10 4FAC for descriptions.				
Offset 0x10 4FD0			*INT_STATUS3*	
Refer to INT_STATUS0 at offset 0x10 4FA0 for descriptions.				
Offset 0x10 4FD4			*INT_ENABLE3*	
Refer to INT_ENABLED0 at offset 0x10 4FA4 for descriptions.				
Offset 0x10 4FD8			*INT_CLEAR3*	
Refer to INT_CLEAR0 at offset 0x10 4FA8 for descriptions.				
Offset 0x10 4FDC			*INT_SET3*	
Refer to INT_SET0 at offset 0x10 4FAC for descriptions.				

GPIO REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
GPIO Module Status Register for the 12 Timestamp Units (TSU)				
Offset 0x10 4FE0			*INT_STATUS4*	
31:24		-	Unused	
23	R	0	INT_OE_11	Internal overrun error in TSU11. Data in TSU overwritten before read by CPU (i.e., before DATA_VALID interrupt was cleared).
22	R	0	INT_OE_10	Internal overrun error in TSU10. Data in TSU overwritten before read by CPU (i.e., before DATA_VALID interrupt was cleared).
21	R	0	INT_OE_9	Internal overrun error in TSU9. Data in TSU overwritten before read by CPU (i.e., before DATA_VALID interrupt was cleared).
20	R	0	INT_OE_8	Internal overrun error in TSU8. Data in TSU overwritten before read by CPU (i.e., before DATA_VALID interrupt was cleared).
19	R	0	INT_OE_7	Internal overrun error in TSU7. Data in TSU overwritten before read by CPU (i.e., before DATA_VALID interrupt was cleared).
18	R	0	INT_OE_6	Internal overrun error in TSU6. Data in TSU overwritten before read by CPU (i.e., before DATA_VALID interrupt was cleared).
17	R	0	INT_OE_5	Internal overrun error in TSU5. Data in TSU overwritten before read by CPU (i.e., before DATA_VALID interrupt was cleared).
16	R	0	INT_OE_4	Internal overrun error in TSU4. Data in TSU overwritten before read by CPU (i.e., before DATA_VALID interrupt was cleared).
15	R	0	INT_OE_3	Internal overrun error in TSU3. Data in TSU overwritten before read by CPU (i.e., before DATA_VALID interrupt was cleared).
14	R	0	INT_OE_2	Internal overrun error in TSU2. Data in TSU overwritten before read by CPU (i.e., before DATA_VALID interrupt was cleared).
13	R	0	INT_OE_1	Internal overrun error in TSU1. Data in TSU overwritten before read by CPU (i.e., before DATA_VALID interrupt was cleared).

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GPIO REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
12	R	0	INT_OE_0	Internal overrun error in TSU0. Data in TSU overwritten before read by CPU (i.e., before DATA_VALID interrupt was cleared).
11	R	0	DATA_VALID_11	Data in TSU11 is ready to be read.
10	R	0	DATA_VALID_10	Data in TSU10 is ready to be read.
9	R	0	DATA_VALID_9	Data in TSU9 is ready to be read.
8	R	0	DATA_VALID_8	Data in TSU8 is ready to be read.
7	R	0	DATA_VALID_7	Data in TSU7 is ready to be read.
6	R	0	DATA_VALID_6	Data in TSU6 is ready to be read.
5	R	0	DATA_VALID_5	Data in TSU5 is ready to be read.
4	R	0	DATA_VALID_4	Data in TSU4 is ready to be read.
3	R	0	DATA_VALID_3	Data in TSU3 is ready to be read.
2	R	0	DATA_VALID_2	Data in TSU2 is ready to be read.
1	R	0	DATA_VALID_1	Data in TSU1 is ready to be read.
0	R	0	DATA_VALID_0	Data in TSU0 is ready to be read.
Offset 0x10 4FE4			*INT_ENABLE4*	
31:24		-	Unused	
23	R/W	0	INT_OE_11_EN	Internal overrun interrupt enable register for TSU11: 0 = Interrupt disabled. 1 = Interrupt enabled.
22	R/W	0	INT_OE_10_EN	Internal overrun interrupt enable register for TSU10: 0 = Interrupt disabled. 1 = Interrupt enabled.
21	R/W	0	INT_OE_9_EN	Internal overrun interrupt enable register for TSU9: 0 = Interrupt disabled. 1 = Interrupt enabled.
20	R/W	0	INT_OE_8_EN	Internal overrun interrupt enable register for TSU8: 0 = Interrupt disabled. 1 = Interrupt enabled.
19	R/W	0	INT_OE_7_EN	Internal overrun interrupt enable register for TSU7: 0 = Interrupt disabled. 1 = Interrupt enabled.
18	R/W	0	INT_OE_6_EN	Internal overrun interrupt enable register for TSU6: 0 = Interrupt disabled. 1 = Interrupt enabled.
17	R/W	0	INT_OE_5_EN	Internal overrun interrupt enable register for TSU5: 0 = Interrupt disabled. 1 = Interrupt enabled.
16	R/W	0	INT_OE_4_EN	Internal overrun interrupt enable register for TSU4: 0 = Interrupt disabled. 1 = Interrupt enabled.
15	R/W	0	INT_OE_3_EN	Internal overrun interrupt enable register for TSU3: 0 = Interrupt disabled. 1 = Interrupt enabled.
14	R/W	0	INT_OE_2_EN	Internal overrun interrupt enable register for TSU2: 0 = Interrupt disabled. 1 = Interrupt enabled.

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GPIO REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
13	R/W	0	INT_OE_1_EN	Internal overrun interrupt enable register for TSU1: 0 = Interrupt disabled. 1 = Interrupt enabled.
12	R/W	0	INT_OE_0_EN	Internal overrun interrupt enable register for TSU0: 0 = Interrupt disabled. 1 = Interrupt enabled.
11	R/W	0	DATA_VALID_11_EN	Data valid interrupt enable register for TSU11: 0 = Interrupt disabled. 1 = Interrupt enabled.
10	R/W	0	DATA_VALID_10_EN	Data valid interrupt enable register for TSU10: 0 = Interrupt disabled. 1 = Interrupt enabled.
9	R/W	0	DATA_VALID_9_EN	Data valid interrupt enable register for TSU9": 0 = Interrupt disabled. 1 = Interrupt enabled.
8	R/W	0	DATA_VALID_8_EN	Data valid interrupt enable register for TSU8: 0 = Interrupt disabled. 1 = Interrupt enabled.
7	R/W	0	DATA_VALID_7_EN	Data valid interrupt enable register for TSU7: 0 = Interrupt disabled. 1 = Interrupt enabled.
6	R/W	0	DATA_VALID_6_EN	Data valid interrupt enable register for TSU6: 0 = Interrupt disabled. 1 = Interrupt enabled.
5	R/W	0	DATA_VALID_5_EN	Data valid interrupt enable register for TSU5: 0 = Interrupt disabled. 1 = Interrupt enabled.
4	R/W	0	DATA_VALID_4_EN	Data valid interrupt enable register for TSU4: 0 = Interrupt disabled. 1 = Interrupt enabled.
3	R/W	0	DATA_VALID_3_EN	Data valid interrupt enable register for TSU3: 0 = Interrupt disabled. 1 = Interrupt enabled.
2	R/W	0	DATA_VALID_2_EN	Data valid interrupt enable register for TSU2: 0 = Interrupt disabled. 1 = Interrupt enabled.
1	R/W	0	DATA_VALID_1_EN	Data valid interrupt enable register for TSU1: 0 = Interrupt disabled. 1 = Interrupt enabled.
0	R/W	0	DATA_VALID_0_EN	Data valid interrupt enable register for TSU0: 0 = Interrupt disabled. 1 = Interrupt enabled.
Offset 0x10 4FE8			*INT_CLEAR4*	
31:24		-	Unused	
23	W	0	INT_OE_11_CLR	Active high clear for internal overrun interrupt for TSU11
22	W	0	INT_OE_10_CLR	Active high clear for internal overrun interrupt for TSU10
21	W	0	INT_OE_9_CLR	Active high clear for internal overrun interrupt for TSU9
20	W	0	INT_OE_8_CLR	Active high clear for internal overrun interrupt for TSU8
19	W	0	INT_OE_7_CLR	Active high clear for internal overrun interrupt for TSU7

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GPIO REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
18	W	0	INT_OE_6_CLR	Active high clear for internal overrun interrupt for TSU6
17	W	0	INT_OE_5_CLR	Active high clear for internal overrun interrupt for TSU5
16	W	0	INT_OE_4_CLR	Active high clear for internal overrun interrupt for TSU4
15	W	0	INT_OE_3_CLR	Active high clear for internal overrun interrupt for TSU3
14	W	0	INT_OE_2_CLR	Active high clear for internal overrun interrupt for TSU2
13	W	0	INT_OE_1_CLR	Active high clear for internal overrun interrupt for TSU1
12	W	0	INT_OE_0_CLR	Active high clear for internal overrun interrupt for TSU0
11	W	0	DATA_VALID_11_CLR	Active high clear for data valid interrupt for TSU11
10	W	0	DATA_VALID_10_CLR	Active high clear for data valid interrupt for TSU10
9	W	0	DATA_VALID_9_CLR	Active high clear for data valid interrupt for TSU9
8	W	0	DATA_VALID_8_CLR	Active high clear for data valid interrupt for TSU8
7	W	0	DATA_VALID_7_CLR	Active high clear for data valid interrupt for TSU7
6	W	0	DATA_VALID_6_CLR	Active high clear for data valid interrupt for TSU6
5	W	0	DATA_VALID_5_CLR	Active high clear for data valid interrupt for TSU5
4	W	0	DATA_VALID_4_CLR	Active high clear for data valid interrupt for TSU4
3	W	0	DATA_VALID_3_CLR	Active high clear for data valid interrupt for TSU3
2	W	0	DATA_VALID_2_CLR	Active high clear for data valid interrupt for TSU2
1	W	0	DATA_VALID_1_CLR	Active high clear for data valid interrupt for TSU1
0	W	0	DATA_VALID_0_CLR	Active high clear for data valid interrupt for TSU0
Offset Offset 0x10 4FEC			*INT_SET4*	
31:24		-	Unused	
23	W	0	INT_OE_11_SET	Active high set for internal overrun interrupt for TSU11
22	W	0	INT_OE_10_SET	Active high set for internal overrun interrupt for TSU10
21	W	0	INT_OE_9_SET	Active high set for internal overrun interrupt for TSU9
20	W	0	INT_OE_8_SET	Active high set for internal overrun interrupt for TSU8
19	W	0	INT_OE_7_SET	Active high set for internal overrun interrupt for TSU7
18	W	0	INT_OE_6_SET	Active high set for internal overrun interrupt for TSU6
17	W	0	INT_OE_5_SET	Active high set for internal overrun interrupt for TSU5
16	W	0	INT_OE_4_SET	Active high set for internal overrun interrupt for TSU4
15	W	0	INT_OE_3_SET	Active high set for internal overrun interrupt for TSU3
14	W	0	INT_OE_2_SET	Active high set for internal overrun interrupt for TSU2
13	W	0	INT_OE_1_SET	Active high set for internal overrun interrupt for TSU1
12	W	0	INT_OE_0_SET	Active high set for internal overrun interrupt for TSU0
11	W	0	DATA_VALID_11_SET	Active high set for data valid interrupt for TSU11
10	W	0	DATA_VALID_10_SET	Active high set for data valid interrupt for TSU10
9	W	0	DATA_VALID_9_SET	Active high set for data valid interrupt for TSU9
8	W	0	DATA_VALID_8_SET	Active high set for data valid interrupt for TSU8
7	W	0	DATA_VALID_7_SET	Active high set for data valid interrupt for TSU7

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GPIO REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
6	W	0	DATA_VALID_6_SET	Active high set for data valid interrupt for TSU6
5	W	0	DATA_VALID_5_SET	Active high set for data valid interrupt for TSU5
4	W	0	DATA_VALID_4_SET	Active high set for data valid interrupt for TSU4
3	W	0	DATA_VALID_3_SET	Active high set for data valid interrupt for TSU3
2	W	0	DATA_VALID_2_SET	Active high set for data valid interrupt for TSU2
1	W	0	DATA_VALID_1_SET	Active high set for data valid interrupt for TSU1
0	W	0	DATA_VALID_0_SET	Active high set for data valid interrupt for TSU0
Offset 0x10 4FF0			*Reserved*	

GPIO REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
GPIO POWERDOWN				
Offset 0x10 4FF4			*POWERDOWN*	
31	R/W	0	POWERDOWN	0 = Normal operation of peripheral. This is the reset value. 1 = Module is in powerdown and module clock can be removed. Module must respond to all reads. Generate e.g. DEADABBA (except for reads of the powerdown bit) Module should generate ERR ACK on writes (except for writes to the powerdown bit).
30:0		-	Unused	
Offset 0x10 4FF8			*Reserved*	
GPIO Module ID				
Offset 0x10 4FFC			*MODULE_ID*	
31:15	R	0x010F	Module ID	Unique 16-bit code. Module ID 0 and -1 are reserved for future use.
14:12	R	0	MajRev	Major Revision
11:8	R	1	MinRev	Minor Revision
7:0	R	0	Module Aperture Size	Aperture size = 4 kB*(bit_value+1), so 0 means 4 kB (the default).

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MPEG Video Decoder Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.34)

MPEG VIDEO DECODER REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 5000			*VLD_COMMAND*	
31:12		-	Unused	
11:8	R/W	0	Command	Command code of the VLD command to be executed. Refer to *(PNX8526 User Manual, Ref. UM10104_1, Chap.34)* for more information. 0x1 = Shift the bitstream by '"count"' bits. 0x2 = Parse for a given number of macroblocks. 0x3 = Search for the next start code. 0x4 = Reset the MPEG-PIPE. 0x5 = Initialize the VLD. 0x6 = Search for the given start code. 0x7 = Parse one row of macroblocks.
7:0	R/W	0	Mblock/Shift Count or Start Code	For the 'Shift Bitstream' command, only the lower 4 bits are used; the upper 4 bits should be set to 0. All 8 bits are used for the 'Parse macroblocks' and 'Search for given start code' commands.
Offset 0x10 5004			*VLD_SR*	
31:15			Reserved	
15:0	R	NI	Shift Register	This read-only register is a shadow of the VLD's operational shift register. It allows the TM32 CPU core to access the bitstream through the VLD. Bits 0 through 15 are the current bits of the VLD shift register.
Offset 0x10 5008			*VLD_QS*	
31:5		-	Unused	
4:0	R/W	NI	Quant scale	This 5-bit read/write register contains the quantization scale code to be output by the VLD until it is overridden by a macroblock quantizer scale code. The quantizer scale code is part of the macroblock header output.
Offset 0x10 500C			*VLD_PI*	
31:28	R/W	NI	Vertical back.rsize	No. of bits per backward vertical motion vector residual in the picture
27:24	R/W	NI	Horizontal back.rsize	No. of bits per backward horizontal motion vector residual in No. picture
23:20	R/W	NI	Vertical for.rsize	No. of bits per forward vertical motion vector residual in picture
19:16	R/W	NI	Horizontal for.rsize	No. of bits per forward horizontal motion vector residual in picture
15		-	Unused	
14	R/W	NI	no_backward	Controls use of backward prediction in macroblocks with bi-directional motion prediction. 0 = Keep backward prediction. 1 = Drop backward prediction.
13	R/W	NI	mpeg2mode	0 = The current sequence is MPEG1. 1 = The current sequence is MPEG2. Note: For error checking only
12	R/W	NI	no_uv_yhalf	Controls use of vertical half-pel flag for UV component in all macroblocks of a B picture. 0 = Keep UV vertical half-pel flag. 1 = Drop UV vertical half-pel flag.

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MPEG VIDEO DECODER REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
11	R/W	NI	no_y_yhalf	Controls use of vertical half-pel flag for Y component in all macroblocks of a B picture. 0 = Keep Y vertical half-pel flag 1 = Drop Y vertical half-pel flag
10	R/W	NI	top_field_first	0 = Capture bottom field first. 1= Capture top field first.
9	R/W	NI	full_pel_backward	0 = Backward motion vectors in a picture have half-pel units. 1 = Backward motion vectors in a picture have full-pel units.
8	R/W	NI	full_pel_forward	0 = Forward motion vectors in a picture have half-pel units. 1 = Forward motion vectors in a picture have full-pel units.
7	R/W	NI	half_res_mode	0 = full_res_mode 1 = half_res_mode
6	R/W	NI	mv_concealment	Indicates whether motion vectors are coded in all intra macroblock headers of a picture. 0 = Forward motion vectors are not coded. 1 = Forward motion vectors are coded.
5	R/W	NI	intra_vlc	0 = Use DCT table zero. 1 = Use DCT table one.
4	R/W	NI	frame_prediction_frame_dct	0 = motion_type and dct_type follow the decoded values in the mb_header from the VLD. 1 = motion_type = FRAME, and dct_type = 0. CPU should set it to 0 for Field Pictures and 1 for MPEG1.
3:2	R/W	NI	picture_structure	0x1 = Top-field 0x2 = Bottom-field 0x3 = Frame picture 0x0 = Reserved
1:0	R/W	NI	picture_type	1=I 2=P 3=B 0=D (MPEG1 only)
Offset 0x10 5010			*VLD_MC_STATUS*	
31:24		-	Unused	
23	R	0	DONE_FLUSH	1 signals the completion of the last flush command. CPU writes 1 to this field to acknowledge condition and clear this flag.
22	R/W	0	EOR_ERRCON	1 signals the completion of the last error concealment command. CPU writes 1 to this field to acknowledge condition and clear the flag
21:16	R	0	mc_error_flags	MC error code. 000000 = No error 000001 = Invalid motion type 000010 = Invalid macroblock address increment (>1) 000100 = Macroblock overflow 001000 = Reserved 010000 = Pre-fetch coordinates out of bound 100000 = No prediction for B skipped macroblocks
15:8		-	Unused	
7	RW	0	Time-out	1 = MPEG-PIPE timed out. Refer to*(PNX8526 User Manual, Ref. UM10104_1, Chap.34)*for details on the timeout mechanism. Bit is cleared by writing a logic ‘1.’

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MPEG VIDEO DECODER REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
6	RW	0	RL overflow	1 = Overflow of run/level values within a block. Refer to*(PNX8526 User Manual, Ref. UM10104_1, Chap.34)* for details on the error handling procedure. This bit is cleared by writing a logic '1' to it.
5:4		-	Unused	
3	RW	0	DMA input done	Conditions for setting this bit depend on the value of the DMA_Input_Done field in the VLD_CTL register. Refer to *(PNX8526 User Manual, Ref. UM10104_1, Chap.34)* for details. This bit is cleared by writing a logic '1' to it.
2	RW	0	Bitstream error	1 = VLD encountered an illegal Huffman code or an unexpected start code. Refer to*(PNX8526 User Manual, Ref. UM10104_1, Chap.34)* for details on the error handling procedure. This bit is cleared by writing a logic '1' to it.
1	RW	0	Start code detected	1 = VLD encountered 0x000001 while executing current command. This bit is cleared by writing a logic '1' to it.
0	R		VLD Command done	1 = Successful completion of current command. This bit is cleared by issuing a new command.
Offset 0x10 5014			*VLD_IE*	
31:24		-	Unused	
23	R/W	0	DONE_FLUSH_IE	This bit enables the matching bit from the status register 0x010 to issue an IR to the CPU.
22	R/W	0	EOR_ERRCON_IE	This bit enables the matching bit from the status register 0x010 to issue an IR to the CPU.
21:16	R/W	0	MC Int. Enables	Each bit enables the matching bit from the status register 0x010 to issue an IR to the CPU.
15:8		-	Unused	
7:0	R/W	0	VLD Int. Enables	Each bit enables the matching bit from the status register 0x010 to issue an IR to the CPU.
Offset 0x10 5018			*VLD_CTL*	
31:17		-	Unused	
16	W	0	slice_start_code_strobe	When CPU writes 1 to this field, the VLD copies the value of slice_start_code to its internal register. CPU should do this only when the VLD is stopped. This bit is always read as 0.
15:8	R/W	0	slice start code	Slice start code when the VLD is restarted; the slice_start_code_ strobe bit field must be set to '1' in order to update this field.
7:3		-	Unused	
2	R/W	0	DMA-input-done-mode	0 = VLD sets the DMA_INPUT_DONE flag (in VLD_MC_STATUS register) when the DMA_INP_CNT transitions from non-zero to zero. 1 = The same flag is set only with the additional condition that both highway input buffers are empty. The slice_start_code_strobe bit field must be set to '0' in order to update this field.
1:0		-	Unused	
Offset 0x10 501C			*VLD_INP_ADR*	
31:0	R/W	NI	VLD Input Memory Address	Memory address from which the VLD is reading (updated when DMA read transfer is completed.)
Offset 0x10 5020			*VLD_INP_CNT*	
31:15		-	Unused	

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MPEG VIDEO DECODER REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
14:0	R/W	0	VLD Input Count	Number of bytes to be read from main memory
Offset 0x10 5024—5030			*UNUSED*	
Offset 0x10 5034			*VLD_BIT_CNT*	
31:18		-	Unused	
17:0	R	0	Actual Bit Count	Number of bits consumed by the VLD. Counts upward when bits are shifted out and consumed by the VLD. This counter wraps around after reaching the maximum value. Value can be initialized to zero by issuing the 'Initialize VLD' command.
Offset 0x10 5038			*LINE_SIZE*	
31:13		-	Unused	
12:3	R/W	0	Line size	The line size must be a multiple of 8 bytes. Recommended values are: 320, 352, 368, 640, 704, 720, 960, 1280, 1440, 1920. LINE_SIZE cannot be 512, 680, 1024, 1360, 1368, 1536, 2040
2:0	R/W	0	Line size	Always 0.
Offset 0x10 5040			*W_TBL0_W0*	
31:24	R/W	NI	w[0][0][3]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 040 to 07C show either the default_intra_matrix or the downloaded_intra_matrix.
23:16	R/W	NI	w[0][0][2]	
15:8	R/W	NI	w[0][0][1]	
7:0	R/W	NI	w[0][0][0]	
Offset 0x10 5044			*W_TBL0_W1*	
31:24	R/W	NI	w[0][0][7]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 040 to 07C show either the default_intra_matrix or the downloaded_intra_matrix.
23:16	R/W	NI	w[0][0][6]	
15:8	R/W	NI	w[0][0][5]	
7:0	R/W	NI	w[0][0][4]	
Offset 0x10 5048			*W_TBL0_W2*	
31:24	R/W	NI	w[0][1][3]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 040 to 07C show either the default_intra_matrix or the downloaded_intra_matrix.
23:16	R/W	NI	w[0][1][2]	
15:8	R/W	NI	w[0][1][1]	
7:0	R/W	NI	w[0][1][0]	
Offset 0x10 504C			*W_TBL0_W3*	
31:24	R/W	NI	w[0][1][7]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 040 to 07C show either the default_intra_matrix or the downloaded_intra_matrix.
23:16	R/W	NI	w[0][1][6]	
15:8	R/W	NI	w[0][1][5]	
7:0	R/W	NI	w[0][1][4]	
Offset 0x10 5050			*W_TBL0_W4*	
31:24	R/W	NI	w[0][2][3]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 040 to 07C show either the default_intra_matrix or the downloaded_intra_matrix.
23:16	R/W	NI	w[0][2][2]	
15:8	R/W	NI	w[0][2][1]	
7:0	R/W	NI	w[0][2][0]	
Offset 0x10 5054			*W_TBL0_W5*	

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MPEG VIDEO DECODER REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
31:24	R/W	NI	w[0][2][7]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 040 to 07C show either the default_intra_matrix or the downloaded_intra_matrix.
23:16	R/W	NI	w[0][2][6]	
15:8	R/W	NI	w[0][2][5]	
7:0	R/W	NI	w[0][2][4]	
Offset 0x10 5058			*W_TBL0_W6*	
31:24	R/W	NI	w[0][3][3]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 040 to 07C show either the default_intra_matrix or the downloaded_intra_matrix.
23:16	R/W	NI	w[0][3][2]	
15:8	R/W	NI	w[0][3][1]	
7:0	R/W	NI	w[0][3][0]	
Offset 0x10 505C			*W_TBL0_W7*	
31:24	R/W	NI	w[0][3][7]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 040 to 07C show either the default_intra_matrix or the downloaded_intra_matrix.
23:16	R/W	NI	w[0][3][6]	
15:8	R/W	NI	w[0][3][5]	
7:0	R/W	NI	w[0][3][4]	
Offset 0x10 5060			*W_TBL0_W8*	
31:24	R/W	NI	w[0][4][3]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 040 to 07C show either the default_intra_matrix or the downloaded_intra_matrix.
23:16	R/W	NI	w[0][4][2]	
15:8	R/W	NI	w[0][4][1]	
7:0	R/W	NI	w[0][4][0]	
Offset 0x10 5064			*W_TBL0_W9*	
31:24	R/W	NI	w[0][4][7]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 040 to 07C show either the default_intra_matrix or the downloaded_intra_matrix.
23:16	R/W	NI	w[0][4][6]	
15:8	R/W	NI	w[0][4][5]	
7:0	R/W	NI	w[0][4][4]	
Offset 0x10 5068			*W_TBL0_W10*	
31:24	R/W	NI	w[0][5][3]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 040 to 07C show either the default_intra_matrix or the downloaded_intra_matrix.
23:16	R/W	NI	w[0][5][2]	
15:8	R/W	NI	w[0][5][1]	
7:0	R/W	NI	w[0][5][0]	
Offset 0x10 506C			*W_TBL0_W11*	
31:24	R/W	NI	w[0][5][7]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 040 to 07C show either the default_intra_matrix or the downloaded_intra_matrix.
23:16	R/W	NI	w[0][5][6]	
15:8	R/W	NI	w[0][5][5]	
7:0	R/W	NI	w[0][5][4]	

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MPEG VIDEO DECODER REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 5070			*W_TBL0_W12*	
31:24	R/W	NI	w[0][6][3]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 040 to 07C show either the default_intra_matrix or the downloaded_intra_matrix.
23:16	R/W	NI	w[0][6][2]	
15:8	R/W	NI	w[0][6][1]	
7:0	R/W	NI	w[0][6][0]	
Offset 0x10 5074			*W_TBL0_W13*	
31:24	R/W	NI	w[0][6][7]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 040 to 07C show either the default_intra_matrix or the downloaded_intra_matrix.
23:16	R/W	NI	w[0][6][6]	
15:8	R/W	NI	w[0][6][5]	
7:0	R/W	NI	w[0][6][4]	
Offset 0x10 5078			*W_TBL0_W14*	
31:24	R/W	NI	w[0][7][3]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 040 to 07C show either the default_intra_matrix or the downloaded_intra_matrix.
23:16	R/W	NI	w[0][7][2]	
15:8	R/W	NI	w[0][7][1]	
7:0	R/W	NI	w[0][7][0]	
Offset 0x10 507C			*W_TBL0_W15*	
31:24	R/W	NI	w[0][7][7]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 040 to 07C show either the default_intra_matrix or the downloaded_intra_matrix.
23:16	R/W	NI	w[0][7][6]	
15:8	R/W	NI	w[0][7][5]	
7:0	R/W	NI	w[0][7][4]	
Offset 0x10 5080			*W_TBL1_W0*	
31:24	R/W	NI	w[1][0][3]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 080 to 0BC show either the default_non_intra_matrix or downloaded_non_intra_matrix.
23:16	R/W	NI	w[1][0][2]	
15:8	R/W	NI	w[1][0][1]	
7:0	R/W	NI	w[1][0][0]	
Offset 0x10 5084			*W_TBL1_W1*	
31:24	R/W	NI	w[1][0][7]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 080 to 0BC show either the default_non_intra_matrix or downloaded_non_intra_matrix.
23:16	R/W	NI	w[1][0][6]	
15:8	R/W	NI	w[1][0][5]	
7:0	R/W	NI	w[1][0][4]	
Offset 0x10 5088			*W_TBL1_W2*	
31:24	R/W	NI	w[1][1][3]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 080 to 0BC show either the default_non_intra_matrix or downloaded_non_intra_matrix.
23:16	R/W	NI	w[1][1][2]	
15:8	R/W	NI	w[1][1][1]	
7:0	R/W	NI	w[1][1][0]	
Offset 0x10 508C			*W_TBL1_W3*	

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MPEG VIDEO DECODER REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
31:24	R/W	NI	w[1][1][7]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 080 to 0BC show either the default_non_intra_matrix or downloaded_non_intra_matrix.
23:16	R/W	NI	w[1][1][6]	
15:8	R/W	NI	w[1][1][5]	
7:0	R/W	NI	w[1][1][4]	
Offset 0x10 5090			*W_TBL1_W4*	
31:24	R/W	NI	w[1][2][3]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 080 to 0BC show either the default_non_intra_matrix or downloaded_non_intra_matrix.
23:16	R/W	NI	w[1][2][2]	
15:8	R/W	NI	w[1][2][1]	
7:0	R/W	NI	w[1][2][0]	
Offset 0x10 5094			*W_TBL1_W5*	
31:24	R/W	NI	w[1][2][7]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 080 to 0BC show either the default_non_intra_matrix or downloaded_non_intra_matrix.
23:16	R/W	NI	w[1][2][6]	
15:8	R/W	NI	w[1][2][5]	
7:0	R/W	NI	w[1][2][4]	
Offset 0x10 5098			*W_TBL1_W6*	
31:24	R/W	NI	w[1][3][3]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 080 to 0BC show either the default_non_intra_matrix or downloaded_non_intra_matrix.
23:16	R/W	NI	w[1][3][2]	
15:8	R/W	NI	w[1][3][1]	
7:0	R/W	NI	w[1][3][0]	
Offset 0x10 509C			*W_TBL1_W7*	
31:24	R/W	NI	w[1][3][7]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 080 to 0BC show either the default_non_intra_matrix or downloaded_non_intra_matrix.
23:16	R/W	NI	w[1][3][6]	
15:8	R/W	NI	w[1][3][5]	
7:0	R/W	NI	w[1][3][4]	
Offset 0x10 50A0			*W_TBL1_W8*	
31:24	R/W	NI	w[1][4][3]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 080 to 0BC show either the default_non_intra_matrix or downloaded_non_intra_matrix.
23:16	R/W	NI	w[1][4][2]	
15:8	R/W	NI	w[1][4][1]	
7:0	R/W	NI	w[1][4][0]	
Offset 0x10 50A4			*W_TBL1_W9*	
31:24	R/W	NI	w[1][4][7]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 080 to 0BC show either the default_non_intra_matrix or downloaded_non_intra_matrix.
23:16	R/W	NI	w[1][4][6]	
15:8	R/W	NI	w[1][4][5]	
7:0	R/W	NI	w[1][4][4]	

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MPEG VIDEO DECODER REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 50A8			*W_TBL1_W10*	
31:24	R/W	NI	w[1][5][3]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 080 to 0BC show either the default_non_intra_matrix or downloaded_non_intra_matrix.
23:16	R/W	NI	w[1][5][2]	
15:8	R/W	NI	w[1][5][1]	
7:0	R/W	NI	w[1][5][0]	
Offset 0x10 50AC			*W_TBL1_W11*	
31:24	R/W	NI	w[1][5][7]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 080 to 0BC show either the default_non_intra_matrix or downloaded_non_intra_matrix.
23:16	R/W	NI	w[1][5][6]	
15:8	R/W	NI	w[1][5][5]	
7:0	R/W	NI	w[1][5][4]	
Offset 0x10 50B0			*W_TBL1_W12*	
31:24	R/W	NI	w[1][6][3]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 080 to 0BC show either the default_non_intra_matrix or downloaded_non_intra_matrix.
23:16	R/W	NI	w[1][6][2]	
15:8	R/W	NI	w[1][6][1]	
7:0	R/W	NI	w[1][6][0]	
Offset 0x10 50B4			*W_TBL1_W13*	
31:24	R/W	NI	w[1][6][7]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 080 to 0BC show either the default_non_intra_matrix or downloaded_non_intra_matrix.
23:16	R/W	NI	w[1][6][6]	
15:8	R/W	NI	w[1][6][5]	
7:0	R/W	NI	w[1][6][4]	
Offset 0x10 50B8			*W_TBL1_W14*	
31:24	R/W	NI	w[1][7][3]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 080 to 0BC show either the default_non_intra_matrix or downloaded_non_intra_matrix.
23:16	R/W	NI	w[1][7][2]	
15:8	R/W	NI	w[1][7][1]	
7:0	R/W	NI	w[1][7][0]	
Offset 0x10 50BC			*W_TBL1_W15*	
31:24	R/W	NI	w[1][7][7]	The two quantizer matrices that are being used are mapped into MMIO space. Each value in the 8x8 quantizer matrix occupies eight bits. These two matrices take 128 bytes total. Offsets 080 to 0BC show either the default_non_intra_matrix or downloaded_non_intra_matrix.
23:16	R/W	NI	w[1][7][6]	
15:8	R/W	NI	w[1][7][5]	
7:0	R/W	NI	w[1][7][4]	
Offset 0x10 50C0			*IQ_CONTROL*	
31:6		-	Unused	
5:4	R/W	00	Intra_DC_Precision	Used to compute intra_dc_mult and reset values of intra_dc_pred.
3	R/W	0	Default_Non_Intra_Q_Matrix	If set, indicates the non-intra default quantizer matrix is being used.
2	R/W	1	Default_Intra_Q_Matrix	If set, indicates the default intra quantizer matrix is being used
1	R/W	0	Alt_Scan	0 = The Zig-Zag scan table is used for the current block. 1 = The alternate scan table is used.
0	R/W	0	Quant_Scale_Type	This field is used to select the quantizer scale table.

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MPEG VIDEO DECODER REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 50C4			*RL_STATS*	
31:20	R/W	0	Total_Coded_Block_Ct	Total number of coded blocks in multiples of 1024. Can be initialized by writing the required values through MMIO write transaction.
19:0	R/W	0	Total_Symbol_Cnt	Total number of non-zero DCT coefficients in multiples of 1024. This field can be initialized by writing the required values through MMIO write transaction.
Offset 0x10 50C8			*MP_IQ_SEL_0*	
31:0	R/W	0	MP_IQ_SEL_0	The MP_IQ_SEL_0 and MP_IQ_SEL_1 is initialized to zero after hardware or software reset. The coefficient selection scheme is programmable and operates at an 8-by-8 block level. The TM32 CPU core will write 64-bit values into the MP_IQ_SEL_0 and MP_IQ_SEL_1 MMIO registers. Each bit in the MMIO register is used to select either a coefficient value from VLD or a zero coefficient value within an 8-by-8 block. The bit value of '0' selects the coefficient from the VLD and the bit value of '1' selects the zero value.
Offset 0x10 50CC			*MP_IQ_SEL_1*	
31:0	R/W	0	MP_IQ_SEL_1	The MP_IQ_SEL_0 and MP_IQ_SEL_1 is initialized to zero after hardware or software reset. The coefficient selection scheme is programmable and operates at an 8-by-8 block level. The TM32 CPU core will write 64-bit values into the MP_IQ_SEL_0 and MP_IQ_SEL_1 MMIO registers. Each bit in the MMIO register is used to select either a coefficient value from VLD or a zero coefficient value within an 8-by-8 block. The bit value of '0' selects the coefficient from the VLD and the bit value of '1' selects the zero value.
Offset 0x10 5200			*MC_PICINFO0*	
31		-	Unused	
30:24	R/W	NI	mb_row_offset	Starting macroblock row in the decoding picture which is the first macroblock row the current destination field buffers correspond to. For I and P pictures, this number should always be 0 because reference pictures are not allowed to span multiple non-continuous SDRAM buffers. For B pictures, the decoding picture is allowed to span multiple non-continuous SDRAM buffers. This offset allows the Storage Unit to compute the correct storage coordinates in the current destination buffers.
23:20		-	Unused	
19:16	R/W	NI	mc_timeout_period	If non-zero VLD interrupts the CPU if no macroblocks are stored in SDRAM by the MC within mc_timeout_period*2048 CPU cycles while the VLD is in parsing mode. 0 has no effect.
15:8	R/W	NI	mb_height	Number of luminance (Y) macroblocks per column in a frame picture, which is a fixed number for a given video sequence. The MC relies on this number to detect out-of-bounds reference errors.
7:0	R/W	NI	mb_width	Number of macroblocks per row in a picture in the current sequence
Offset 0x10 5208			*MC_PICINFO2*	
31:24	R/W	NI	err_end_mb_row	Ending macroblock row in error concealment (for each errcon2_cmd)
23:16	R/W	NI	err_end_mb_col	Ending macroblock column in error concealment (for each errcon2_cmd)
15:8	R/W	NI	err_mb_row	Macroblock row-to-start error concealment (for each errcon1_cmd or errcon2_cmd)

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MPEG VIDEO DECODER REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
7:0	R/W	NI	err_mb_col	Macroblock column-to-start error concealment (for each errcon1_cmd or errcon2_cmd)
Offset 0x10 520C			*MC_FREFY0*	
31:0	R/W	NI	fb_fref_Y_f0	SDRAM base address of forward reference top-field buffer for the Y component
Offset 0x10 5210			*MC_FREFY1*	
31:0	R/W	NI	fb_fref_Y_f1	SDRAM base address of forward reference bottom-field buffer for the Y component
Offset 0x10 5214			*MC_FREFUV0*	
31:0	R/W	NI	fb_fref_UV_f0	SDRAM base address of forward reference top-field buffer for the UV component
Offset 0x10 5218			*MC_FREFUV1*	
31:0	R/W	NI	fb_fref_UV_f1	SDRAM base address of forward reference bottom-field buffer for the UV component
Offset 0x10 521C			*MC_BREFY0*	
31:0	R/W	NI	fb_bref_Y_f0	SDRAM base address of backward reference top-field buffer for the Y component
Offset 0x10 5220			*MC_BREFY1*	
31:0	R/W	NI	fb_bref_Y_f1	SDRAM base address of backward reference bottom-field buffer for the Y component
Offset 0x10 5224			*MC_BREFUV0*	
31:0	R/W	NI	fb_bref_UV_f0	SDRAM base address of backward reference top-field buffer for the UV component
Offset 0x10 5228			*MC_BREFUV1*	
31:0	R/W	NI	fb_bref_UV_f1	SDRAM base address of backward reference bottom-field buffer for the UV component
Offset 0x10 522C			*MC_DESTY0*	
31:0	R/W	NI	fb_dest_Y_f0	SDRAM base address of destination top-field buffer for the Y component
Offset 0x10 5230			*MC_DESTY1*	
31:0	R/W	NI	fb_dest_Y_f1	SDRAM base address of destination bottom-field buffer for the Y component
Offset 0x10 5234			*MC_DESTUV0*	
31:0	R/W	NI	fb_dest_UV_f0	SDRAM base address of destination top-field buffer for the UV component
Offset 0x10 5238			*MC_DESTUV1*	
31:0	R/W	NI	fb_dest_UV_f1	SDRAM base address of destination bottom-field buffer for the UV component
Offset 0x10 523C			*MC_COMMAND*	
31:3		-	Unused	

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MPEG VIDEO DECODER REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
2:0	R/W	0	mc_cmd	The CPU instructs the MC to perform certain special operations with this command. Refer to MC Command codes for a description. 000 = cmd_done 001 = flush_cmd 010 = errcon1_cmd 100 = errcon2_cmd
Offset 0x10 5240			*MC_PFCOUNT*	
31:16	R/W	0000	count_24x5	Records the total number of 24x5 2-D memory fetches generated.
15:0	R/W	0000	count_24x4	Records the total number of 24x4 2-D memory fetches generated.
Offset 0x10 5244			*MC_STATUS*	
31:24		-	Unused	
23:16	R	NI	start_mb_col	Macroblock column position in the decoding picture where the current slice starts
15:8	R	0	state_mb_row	Macroblock row position in the decoding picture where the last reconstructed macroblock is stored in SDRAM
7:0	R	0	state_mb_col	Macroblock column position in the decoding picture where the last reconstructed macroblock is stored in SDRAM
Offset 0x10 5FF4			*POWERDOWN*	
31:0	R/W	0	PD	MPEG Powerdown indicator 1 = Powerdown 0 = Power up When this bit equals 1, no other registers are accessible.
Offset 0x10 5FFC			*MODULE_ID*	
31:16	R	0x0100	Module ID	MPEG Video Decoder Module ID register
15:12	R	0	MajRev	Major Revision
11:8	R	0	MinRev	Minor Revision
7:0		0	Aperture Size [7:0]	Returns 00 = MPEG Video Aperture = 4kB.

VIP 1 Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.26)

VIDEO INPUT PROCESSOR (VIP) 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
VIP 1 Registers (Offset 0x10 6000) and VIP 2 Registers (Offset 0x10 7000) The VIP 1 (0x10 6000) and 2 (0x10 7000) registers are identical except for their offsets. A duplicate set has been created to facilitate programming. The tables for VIP 2 (0x10 7000) registers follow this table.				
Operating Mode Control Registers				
Offset 0x10 6000			*VIP Mode Control*	
31:30	R/W	0	VID_CFEN[1:0]	Video window capture field enable 00 = Capture disabled. 01 = Capture odd only. 10 = Capture even only. 11 = Capture both.

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VIDEO INPUT PROCESSOR (VIP) 1 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
29	R/W	0	VID_OSM	Video capture one shot mode 0 = Continuously capture fields selected by CFEN. 1 = Capture fields selected by CFEN only once.
28	R/W	0	VID_FSEQ	Video capture field sequence 0 = Capture fields starting with any field. 1 = Capture fields starting with odd field. Setting has no effect unless VID_CFEN is set to capture both.
27:26	R/W	0	AUX_CFEN[1:0]	Auxiliary window capture enable 00 = Capture disabled. 01 = Capture odd only. 10 = Capture even only. 11 = Capture both.
25	R/W	0	AUX_OSM	Auxiliary capture one shot mode 0 = When auxiliary wrap event is reached, buffer wraps around. 1 = When auxiliary wrap event is reached, capturing stops.
24	R/W	0	AUX_FSEQ	Auxiliary capture field sequence 0 = Capture fields starting with any field. 1 = Capture fields starting with odd field. Setting has no effect unless AUX_CFEN is set to capture both.
23:22	R/W	0	AUX_ANC[1:0]	ANC data capture enable 00 = No ANC data captured. 01 = Capture ANC blocks with DID=55 (odd field VBI data). 10 = Capture ANC blocks with DID=91 (even field VBI data). 11 = Capture ANC blocks with DID=91 and 55.
21	R/W	0	AUX_RAW	Auxiliary raw capture enable 0 = Raw capture disabled. 1 = Raw capture enabled, all samples will be captured. When enabled, AUX_ANC and AUX_CFEN settings are ignored.
20:18		-	Unused	
17	R/W	0	RST_ON_ERR	Reset on error. Writing a one will automatically reset the block in case of a pipeline error (e.g., illegal scaling ratio / FIFO overflow).
16	W	0	SOFT_RESET	Soft reset. Writing a one into this bit will reset the block.
15		-	Unused	
14	R/W	0	IFF_CLAMP	Clamp mode for IFF (affects U/V only). 0 = Clamp to 0-255. 1 = Clamp to 16 - 240 (CCIR range).
13:12	R/W	0	IFF_MODE	Interpolation mode 00 = Bypass 01 = Reserved 10 = Co-sited 11 = Interspersed
11		-	Unused	
10	R/W	0	DFF_CLAMP	Clamp mode for DFF (affects U/V only). 0 = Clamp to 0-255. 1 = Clamp to 16 - 240 (CCIR range).
9:8	R/W	0	DFF_MODE	Decimation mode 00 = Bypass 01 = Co-sited (subsample) 10 = Co-sited (lowpass) 11 = Interspersed
7:4		-	Unused	

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VIDEO INPUT PROCESSOR (VIP) 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
3	R/W	0	HSP_CLAMP	Clamp mode for HSP 0 = Clamp to 0-255. 1 = Clamp to CCIR range defined by bit 2.
2	R/W	0	HSP_RGB	Color space mode, defines CCIR clamping range for HSP 0 = Processing in YUV color space 1 = Processing in RGB color space
1:0	R/W	0	HSP_MODE	Horizontal processing mode 00 = Bypass mode 01 = Color space matrix mode 10 = Normal polyphase mode 11 = Transposed polyphase mode
Video Information Registers				
Offset 0x10 6040			*VIP Line Threshold*	
31:11		-	Unused	
10:0	R/W	0	LCTHR[10:0]	Video Line Count Threshold. Line threshold status bit is set if video line count (SVLC) reaches this value.

VIDEO INPUT PROCESSOR (VIP) 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Input Format Control Registers				
Offset 0x10 6100			*Video Input Format*	
31:30	R/W	0	VSRA[1:0]	Video stream realignment 00 = Normal 01 = Ignore 1st sample after HREF. 1x = Reserved
29:21		-	Unused	
20	R/W	0	NHDAUX	Header detect during AUX window 0 = D1 header detection enabled inside AUX window. 1 = D1 header detection disabled inside AUX window.
19	R/W	0	NPAR	Parity check disable 0 = Parity check enabled for D1 header detection. 1 = Parity check disabled for D1 header detection.
18:16		-	Unused	
15:14	R/W	0	VSEL[1:0]	Video source select 00 = Reserved 01 = Video port, encoded sync (D1-Mode) 10 = Video port, external sync (VMI-Mode) 11 = Reserved
13	R/W	0	TWOS	UV data type 0 = Offset binary 1 = Two's complement
12	R/W	0	TPG	Test pattern generator 0 = Video stream selected by VSEL. 1 = Internal test pattern generator
11:10		-	Unused	

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VIDEO INPUT PROCESSOR (VIP) 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
10	R/W	0	FREF	Field toggle reference mode 0 = Normal, use VREF. 1 = Toggling Field bit is used as vertical reference.
9	R/W	0	FTGL	Field toggle mode 0 = Normal 1 = Free toggle (sequence starts with FID = 0).
8:4		-	Unused	
3	R/W	0	SF	Swap field interpretation 0 = Odd (first) field = 0, even (second) field = 1 1 = Odd (first) field = 1, even (second) field = 0
2	R/W	0	FZERO	Force FID value to zero 0 = Field identifier derived from input stream. 1 = Force field identifier value to 0
1	R/W	0	REVS	Vertical sync reference edge 0 = Falling edge / start of active video 1 = Rising edge / end of active video
0	R/W	0	REHS	Horizontal sync reference edge 0 = Falling edge / SAV 1 = Rising edge / EAV
Offset 0x10 6104			*Video Test Pattern Generator Control*	
31	R/W	0	PAL	Field generation mode 0 = NTSC timing 1 = PAL timing
30		-	Unused	
29	R/W	0	VSEL	Vertical timing signal select 0 = Generate VREF. 1 = Generate VS.
28	R/W	0	HSEL	Horizontal timing signal select 0 = Generate HREF. 1 = Generate HS.
27	R/W	0	SWAP	Alternative test pattern 0 = Normal test pattern 1 = Test pattern with diagonal patterns, etc.
26	R/W	0	MOVE	Scrolling enabled for alternative test pattern. 0 = No scrolling 1 = Scrolling enabled.
25:0		-	Unused	
Video Acquisition Window Control Registers				
Offset 0x10 6140			*Video Acquisition Window Start*	
31:27		-	Unused	
26:16	R/W	0	VID_XWS[10:0]	Horizontal video window start The pixel co-sited with the reference edge REHS is numbered 0.
15:11		-	Unused	
10:0	R/W	0	VID_YWS[10:0]	Vertical video window start The first line indicated by the reference edge REVS is numbered 0.
Offset 0x10 6144			*Video Acquisition Window End*	
31:27		-	Unused	

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VIDEO INPUT PROCESSOR (VIP) 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
26:16	R/W	0	VID_XWE[10:0]	Horizontal video window end pixels from XWS up to and including XWE are processed.
15:11		-	Unused	
10:0	R/W	0	VID_YWE[10:0]	Vertical video window end lines from YWS up to and including YWE are processed.
VBI Acquisition Window Control Registers				
Offset 0x10 6180			*Auxiliary Acquisition Window Start*	
31:27		-	Unused	
26:16	R/W	0	AUX_XWS[10:0]	Horizontal auxiliary window start. The pixel co-sited with the reference edge REHS is numbered 0.
15:11		-	Unused	
10:0	R/W	0	AUX_YWS[10:0]	Vertical auxiliary window start. The line co-sited with the reference edge REVS is numbered 0.
Offset 0x10 6184			*Auxiliary Acquisition Window End*	
31:27		-	Unused	
26:16	R/W	0	AUX_XWE[10:0]	Horizontal auxiliary window end pixels from XWS up to and including XWE are processed.
15:11		-	Unused	
10:0	R/W	0	AUX_YWE[10:0]	Vertical auxiliary window end lines from YWS up to and including YWE are processed.

VIDEO INPUT PROCESSOR (VIP) 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Horizontal Video Processing Control Registers				
Offset 0x10 6200			*Initial Zoom*	
31:29	R/W	0	HSP_PHASE_MODE[2:0]	Phase mode 0 = 64 phases 1 = 32 phases 2 = 16 phases 3 = 8 phases 4 = 4 phases 5 = 2 phases 6 = Fixed phase 7 = Linear phase interpolation (only valid for 4 component mode)
28:27		-	Unused	
26	R/W		HSP_FIR_COMP[1:0]	Horizontal filter components 0 = three components, 6-tap FIR each 1 = four components, 3-tap FIR each (4th component unused). In color space matrix mode this value has to remain zero.
25:20		-	Unused	

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VIDEO INPUT PROCESSOR (VIP) 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
19:0	R/W	0	HSP_ZOOM_0[19:0]	Initial zoom for 1st pixel in line (unsigned, LSB = 2^{-16}) 2 0000 (hex) = downscale 50%. 1 0000 (hex) = no scaling = 2^{0} 0 8000 (hex) = zoom 2 x (transposed: downscale 50%). Values above 10000 (hex) are not valid in transposed mode.
Offset 0x10 6204			*Phase Control*	
31		-	Unused	
30:28	R/W	0	HSP_QSHIFT[2:0]	Quantization shift control used to change quantization before being multiplied with HSP_MULTIPLY. 100 (bin) = divide by 16. 101 (bin) = divide by 8. 110 (bin) = divide by 4. 111 (bin) = divide by 2. 000 (bin) = multiply by 1. 001 (bin) = multiply by 2. 010 (bin) = multiply by 4. 011 (bin) = multiply by 8. Warning: A value range overflow caused by an improper quantization shift can not be compensated for later by multiplying a HSP_MULTIPLY value below 0.5.
27:26		-	Unused	
25	R/W	0	HSP_QSIGN	Quantization sign bit
24:16	R/W	0	HSP_QMULTIPLY[8:0]	Quantization multiply control used to compensate for different weight sums in transposed polyphase or color space matrix mode, remaining bits are fraction (largest number is 511/512). Value range: $0 \leq m < 1.0$. Instead of using values in the range of $m < 0.5$ the quantization shift HSP_QSHIFT should be modified to gain more precision in the truncated result.
15:13		-	Unused	
12:0	R/W	0	HSP_OFFSET_0	Initial start offset for DTO
Offset 0x10 6208			*Initial Zoom delta*	
31:26		-	Unused	
25:0	R/W	0	HSP_DZOOM_0[25:0]	Initial zoom delta for 1 pixel in line (signed, LSB = 2^{-27}) used for non-constant scaling ratios.
Offset 0x10 620C			*Zoom delta change*	
31:29		-	Unused	
28:0	R/W	0	HSP_DDZOOM[28:0]	Zoom delta change (signed, LSB = 2^{-40}) used for non-constant scaling ratios.

VIDEO INPUT PROCESSOR (VIP) 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Color Space Matrix Registers				
Offset 0x10 6220			*Color space matrix coefficients C_{00} - C_{02}*	
31:30		-	Unused	

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VIDEO INPUT PROCESSOR (VIP) 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
29:20	R/W	0	CSM_C02[9:0]	Coefficient C02 (signed, LSB = 2^{-9})
19:10	R/W	0	CSM_C01[9:0]	Coefficient C01 (signed, LSB = 2^{-9})
9:0	R/W	0	CSM_C00[9:0]	Coefficient C00 (signed, LSB = 2^{-9})
Note: Signed values are represented as two's complement.				
Offset 0x10 6224			*Color space matrix coefficients C_{10} - C_{12}*	
31:30		-	Unused	
29:20	R/W	0	CSM_C12[9:0]	Coefficient C12 (signed, LSB = 2^{-9})
19:10	R/W	0	CSM_C11[9:0]	Coefficient C11 (signed, LSB = 2^{-9})
9:0	R/W	0	CSM_C10[9:0]	Coefficient C10 (signed, LSB = 2^{-9})
Offset 0x10 6228			*Color space matrix coefficients C_{20} - C_{22}*	
31:30		-	Unused	
29:20	R/W	0	CSM_C22[9:0]	Coefficient C22 (signed, LSB = 2^{-9})
19:10	R/W	0	CSM_C21[9:0]	Coefficient C21 (signed, LSB = 2^{-9})
9:0	R/W	0	CSM_C20[9:0]	Coefficient C20 (signed, LSB = 2^{-9})
Offset 0x10 622C			*Color space matrix offset coefficients D_0 - D_2*	
31:29		-	Unused	
28	R/W	0	CSM_D2_TWOS	Offset coefficient D_2 type 0 = Unsigned. 1 = Signed.
27:20	R/W	0	CSM_D2[7:0]	Offset coefficient D_2 (LSB = 2^0)
19		-	Unused	
18	R/W	0	CSM_D1_TWOS	Offset coefficient D_1 type 0 = Unsigned. 1 = Signed.
17:10	R/W	0	CSM_D1[7:0]	Offset coefficient D_1 (LSB = 2^0)
9		-	Unused	
8	R/W	0	CSM_D0_TWOS	Offset coefficient D_0 type 0 = Unsigned. 1 = Signed.
7:0	R/W	0	CSM_D0[7:0]	Offset coefficient D_0 (LSB = 2^0)
Offset 0x10 6230			*Color space matrix offset coefficients E_0 - E_2*	
31:30		-	Unused	
29:20	R/W	0	CSM_E2[9:0]	Offset coefficient E2 (signed, LSB = 2^{-2})
19:10	R/W	0	CSM_E1[9:0]	Offset coefficient E1 (signed, LSB = 2^{-2})
9:0	R/W	0	CSM_E0[9:0]	Offset coefficient E0 (signed, LSB = 2^{-2})

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VIDEO INPUT PROCESSOR (VIP) 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Color Keying Control Registers				
Offset 0x10 6284			*Color Key Components*	
31:24	R/W	0	CKEY_ALPHA	Alpha value. Defines the alpha value to be used for keyed samples.
23:0		-	Unused	

VIDEO INPUT PROCESSOR (VIP) 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Video Output Format Control Registers				
Offset 0x10 6300			*Video Output Format*	
31:30	R/W	0	PSU_BAMODE	Base address mode 00 = Single set (e.g., progressive video source) base 1-3 according to number of planes (plane 1-3) 01 = Reserved 10 = Alternate sets each field (interlaced video source). base 1-3, odd field (plane 1-3) base 4-6, even field (plane 1-3) 11 = Alternate sets each field and frame (double buffer mode). packed modes only, frame index is set to 1 if cfen=0, frame index is incremented after capturing even field before capturing odd, base address byte offset is defined in PSU_OFFSET1 base 1, odd field 1st frame (plane 1 only) base 2, even field 1st frame (plane 1 only) base 3, odd field 2nd frame (plane 1 only) base 4, even field 2nd frame (plane 1 only)
29:14		-	Unused	
13	R/W	0	PSU_ENDIAN	Output format endianness 0 = Same as system endianness 1 = Opposite of system endianness
12		-	Unused	
11:10	R/W	0	PSU_DITHER	Output format dither mode 00 = No dithering 01 = Error dispersion (never reset pattern). 10 = Error dispersion (reset pattern at first capture enable). 11 = Error dispersion (reset pattern every field).
9:8	R/W	0	PSU_ALPHA	Output format alpha mode 00 = No alpha (alpha byte not written). 01 = Alpha byte written, value from CKEY_ALPHA (offset 284). 10 = Reserved 11 = Reserved Setting 00 is ignored if size of alpha component is less than 8 bits.

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VIDEO INPUT PROCESSOR (VIP) 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
7:0	R/W	0	PSU_OPFMT	Output formats 08 (hex) = YUV 4:2:2, semi-planar 0B (hex) = YUV 4:2:2, planar 0F (hex) = RGB or YUV 4:4:4, planar A9 (hex) = Compressed 4/4/4 + (4 bit alpha) AA (hex) = Compressed 4/5/3 + (4 bit alpha) AD (hex) = Compressed 5/6/5 A0 (hex) = Packed YUY2 4:2:2 A1 (hex) = Packed UYVY 4:2:2 E2 (hex) = YUV or RGB 4:4:4 + (8 bit alpha) E3 (hex) = VYU 4:4:4 + (8 bit alpha)
Offset 0x10 6304			*Target Window Size*	
31:27		-	Unused	
26:16	R/W	0	PSU_LSIZE	Line size. Used for horizontal cropping after scaling. 0 = Cropping disabled. 1 = One pixel
15:11		-	Unused	
10:0	R/W	0	PSU_LCOUNT	Line count. Used for vertical cropping after scaling. 0 = Cropping disabled. 1 = One line

VIDEO INPUT PROCESSOR (VIP) 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Video Output Address Generation Control Registers				
Offset 0x10 6340			*Target Base Address #1*	
31:26		-	Unused	
25:3	R/W	0	PSU_BASE1	Base address DMA #1 used depending on PSU_BAMODE setting.
2:0	R/W	0	PSU_OFFSET1	Base address byte offset plane 1 bits define pixel offset within multi pixel 64 bit words (e.g., a 16-bit pixel can be placed on any 16-bit boundary).
Offset 0x10 6344			*Target Line Pitch #1*	
31:15		-	Unused	
14:3	R/W	0	PSU_PITCH1	Line pitch DMA #1. Signed value (two's complement) used for all packed formats and for plane 1.
2:0		-	Unused	
Offset 0x10 6348			*Target Base Address #2*	
31:26		-	Unused	
25:3	R/W	0	PSU_BASE2	Base address DMA #2 used depending on PSU_BAMODE setting.
2:0	R/W	0	PSU_OFFSET2	Base address byte offset plane 2 bits define pixel offset within multi pixel 64 bit words (e.g., a 16-bit pixel can be placed on any 16-bit boundary).
Offset 0x10 634C			*Target Line Pitch #2*	
31:15		-	Unused	

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VIDEO INPUT PROCESSOR (VIP) 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
14:3	R/W	0	PSU_PITCH2	Line pitch DMA #2, signed value (two's complement) used for planes 2 and 3.
2:0		-	Unused	
Offset 0x10 6350			*Target Base Address #3*	
31:26		-	Unused	
25:3	R/W	0	PSU_BASE3	Base address DMA #3 used depending on PSU_BAMODE setting.
2:0	R/W	0	PSU_OFFSET3	Base address byte offset plane 3 bits define pixel offset within multi pixel 64 bit words (e.g., a 16-bit pixel can be placed on any 16-bit boundary).
Offset 0x10 6354			*Target Base Address #4*	
31:26		-	Unused	
25:3	R/W	0	PSU_BASE4	Base address DMA #4 used depending on PSU_BAMODE setting.
2:0		-	Unused	
Offset 0x10 6358			*Target Base Address #5*	
31:26		-	Unused	
25:3	R/W	0	PSU_BASE5	Base address DMA #5 used depending on PSU_BAMODE setting.
2:0		-	Unused	
Offset 0x10 635C			*Target Base Address #6*	
31:26		-	Unused	
25:3	R/W	0	PSU_BASE6	Base address DMA #6 used depending on PSU_BAMODE setting.
2:0		-	Unused	

VIDEO INPUT PROCESSOR (VIP) 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Auxiliary Data Output Format Control Registers				
Offset 0x10 6380			*Auxiliary Capture Output Format*	
31:30		0	AUX_BAMODE	Base address mode 00 = Pitch mode, wrap at end of buffer or window. 01 = Pitch mode, wrap at end of buffer. 10 = Append mode, wrap at end of buffer or window. 11 = Reserved
29:27		-	Unused	
26	R/W	0	AUX_SGNEX	Auxiliary capture sign extension 0 = No sign extension 1 = Sign extension enabled for 10-bit samples.
25	R/W	0	AUX_BPS	Auxiliary capture bits per sample 0 = 8-bit samples 1 = 10-bit samples
24	R/W	0	AUX_SUBSAMPLE	Auxiliary capture subsample 0 = All samples 1 = Luma (even) samples only

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VIDEO INPUT PROCESSOR (VIP) 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
23:22		-	Unused	
21:0	R/W	0	AUX_BZSIZE[21:0]	Auxiliary capture ring buffer size Size of ring buffer in bytes; 0 = unlimited buffer size.
Auxiliary Data Output Address Generation Control Registers				
Offset 0x10 6390			*Auxiliary Capture Base Address*	
31:26		-	Unused	
25:0	R/W	0	AUX_BASE	Auxiliary capture base address. Lower 3 bits define byte offset within 64-bit words. Offset has to be a multiple of the byte per unit size (e.g., a 16-bit unit can be placed on any 16-bit boundary).
Offset 0x10 6394			*Auxiliary Capture Line Pitch*	
31:15		-	Unused	
14:3	R/W	0	AUX_PITCH	Auxiliary capture line pitch - a signed value
2:0		-	Unused	

VIDEO INPUT PROCESSOR (VIP) 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Miscellaneous Registers				
Offset 0x10 6800—69FC			*Coefficient Table Taps 0-5 (Horizontal) (64 entries x 64 bits)*	
63:62		-	Unused	
61:52	W	NI	TAP_5[X][9:0]	Inverted coefficient, tap #5, two's complement
51:42	W	NI	TAP_4[X][9:0]	Inverted coefficient, tap #4, two's complement
41:32	W	NI	TAP_3[X][9:0]	Inverted coefficient, tap #3, two's complement
31:30		-	Unused	
29:20	W	NI	TAP_2[X][9:0]	Inverted coefficient, tap #2, two's complement
19:10	W	NI	TAP_1[X][9:0]	Inverted coefficient, tap #1, two's complement
9:0	W	NI	TAP_0[X][9:0]	Inverted coefficient, tap #0, two's complement

VIDEO INPUT PROCESSOR (VIP) 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Interrupt and Status Control Registers				
Offset 0x10 6FE0			*Interrupt Status*	
31	R	0	STAT_FID_AUX	Field identifier at start of auxiliary window
30	R	0	STAT_FID_VID	Field identifier at start of video window
29	R	0	STAT_FID_VPI	Field identifier at video input port
28		-	Unused	

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VIDEO INPUT PROCESSOR (VIP) 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
27:16	R	0	STAT_LINE_COUNT[11:0]	Source video line count. Refer to *PNX8526 User Manual, Ref. UM10104_1, Chap.26)* for information on how lines are counted.
15:10		-	Unused	
9	R	0	STAT_AUX_OVRFLW	Auxiliary buffer overflow event
8	R	0	STAT_VID_OVRFLW	Video buffer overflow event
7	R	0	STAT_WIN_SEQBRK	Windower sequence break event
6	R	0	STAT_FID_SEQBRK	Field identifier sequence break event
5	R	0	STAT_LINE_THRESH	Line counter threshold reached event
4	R	0	STAT_AUX_WRAP	Auxiliary capture write pointer wrap around event
3	R	0	STAT_AUX_START_IN	Start of auxiliary data acquisition event
2	R	0	STAT_AUX_END_OUT	End of auxiliary data write to memory event
1	R	0	STAT_VID_START_IN	Start of video data acquisition event
0	R	0	STAT_VID_END_OUT	End of video data write to memory event
Offset 0x10 6FE4			*Interrupt Enable*	
31:10		-	Unused	
9	R/W	0	IEN_AUX_OVRFLW	Auxiliary buffer overflow event
8	R/W	0	IEN_VID_OVRFLW	Video buffer overflow event
7	R/W	0	IEN_WIN_SEQBRK	Windower sequence break event
6	R/W	0	IEN_FID_SEQBRK	Field identifier sequence break event
5	R/W	0	IEN_LINE_THRESH	Line counter threshold reached event
4	R/W	0	IEN_AUX_WRAP	Auxiliary capture write pointer wrap around event
3	R/W	0	IEN_AUX_START_IN	Start of auxiliary data acquisition event
2	R/W	0	IEN_AUX_END_OUT	End of auxiliary data write to memory event
1	R/W	0	IEN_VID_START_IN	Start of video data acquisition event
0	R/W	0	IEN_VID_END_OUT	End of video data write to memory event
Offset 0x10 6FE8			*Interrupt Clear*	
31:10		-	Unused	
9	W	0	CLR_AUX_OVRFLW	Auxiliary buffer overflow event
8	W	0	CLR_VID_OVRFLW	Video buffer overflow event
7	W	0	CLR_WIN_SEQBRK	Windower sequence break event
6	W	0	CLR_FID_SEQBRK	Field identifier sequence break event
5	W	0	CLR_LINE_THRESH	Line counter threshold reached event
4	W	0	CLR_AUX_WRAP	Auxiliary capture write pointer wrap around event
3	W	0	CLR_AUX_START_IN	Start of auxiliary data acquisition event
2	W	0	CLR_AUX_END_OUT	End of auxiliary data write to memory event
1	W	0	CLR_VID_START_IN	Start of video data acquisition event
0	W	0	CLR_VID_END_OUT	End of video data write to memory event
Offset 0x10 6FEC			*Interrupt Set*	

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VIDEO INPUT PROCESSOR (VIP) 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
31:10		-	Unused	
9	W	0	SET_AUX_OVRFLW	Auxiliary buffer overflow event
8	W	0	SET_VID_OVRFLW	Video buffer overflow event
7	W	0	SET_WIN_SEQBRK	Windower sequence break event
6	W	0	SET_FID_SEQBRK	Field Identifier sequence break event
5	W	0	SET_LINE_THRESH	Line counter threshold reached event
4	W	0	SET_AUX_WRAP	Auxiliary capture write pointer wrap around event
3	W	0	SET_AUX_START_IN	Start of auxiliary data acquisition event
2	W	0	SET_AUX_END_OUT	End of auxiliary data write to memory event
1	W	0	SET_VID_START_IN	Start of video data acquisition event
0	W	0	SET_VID_END_OUT	End of video data write to memory event
Offset 0x10 6FF4			*POWERDOWN*	
31	R/W	0	POWER_DOWN	Powerdown register for the module 0 = Normal operation of the peripheral. This is the reset value. 1 = Module is powered down and module clock can be removed. At powerdown, module responds to all reads with DEADABBA (except for reads of powerdown bit) and all writes with ERR ACK (except for writes to powerdown bit).
30:0		-	Unused	Ignore during writes and read as zeroes.
Offset 0x10 6FFC			*Module ID*	
31:16	R	0x011A	MOD_ID	Module ID (unique 16-bit code)
15:12	R	0	REV_MAJOR	Major revision counter
11:8	R	1	REV_MINOR	Minor revision counter
7:0	R	0	APP_SIZE	Aperture Size 0 = 4kB

VIP 2 Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.26)

VIDEO INPUT PROCESSOR (VIP) 2 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
VIP 1 Registers (Offset 0x10 6000) and VIP 2 Registers (Offset 0x10 7000) The VIP 1(0x10 6000) and 2 (0x10 7000) registers are identical except for their offsets. A duplicate set has been created to facilitate programming. The tables for VIP 1 registers (0x10 6000) precede this table.				
Operating Mode Control Registers				
Offset 0x10 7000			*VIP Mode Control*	
Video Information Registers				
Offset 0x10 7040			*VIP Line Threshold*	
Input Format Control Registers				
Offset 0x10 7100			*Video Input Format*	

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VIDEO INPUT PROCESSOR (VIP) 2 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x10 7104			*Video Test Pattern Generator Control*	
Video Acquisition Window Control Registers				
Offset 0x10 7140			*Video Acquisition Window Start*	
Offset 0x10 7144			*Video Acquisition Window End*	
VBI Acquisition Window Control Registers				
Offset 0x10 7180			*Auxiliary Acquisition Window Start*	
Offset 0x10 7184			*Auxiliary Acquisition Window End*	
Horizontal Video Processing Control Registers				
Offset 0x10 7200			*Initial Zoom*	
Offset 0x10 7204			*Phase Control*	
Offset 0x10 7208			*Initial Zoom delta*	
Offset 0x10 720C			*Zoom delta change*	
Color Space Matrix Registers				
Offset 0x10 7220			*Color space matrix coefficients C_{00} - C_{02}*	
Offset 0x10 7224			*Color space matrix coefficients C_{10} - C_{12}*	
Offset 0x10 7228			*Color space matrix coefficients C_{20} - C_{22}*	
Offset 0x10 722C			*Color space matrix offset coefficients D_0 - D_2*	
Offset 0x10 7230			*Color space matrix offset coefficients E_0 - E_2*	
Color Keying Control Registers				
Offset 0x10 7284			*Color Key Components*	
Video Output Format Control Registers				
Offset 0x10 7300			*Video Output Format*	
Offset 0x10 7304			*Target Window Size*	
Video Output Address Generation Control Registers				
Offset 0x10 7340			*Target Base Address #1*	
Offset 0x10 7344			*Target Line Pitch #1*	
Offset 0x10 7348			*Target Base Address #2*	
Offset 0x10 734C			*Target Line Pitch #2*	
Offset 0x10 7350			*Target Base Address #3*	
Offset 0x10 7354			*Target Base Address #4*	
Offset 0x10 7358			*Target Base Address #5*	
Offset 0x10 735C			*Target Base Address #6*	
Auxiliary Data Output Format Control Registers				
Offset 0x10 7380			*Auxiliary Capture Output Format*	
Auxiliary Data Output Address Generation Control Registers				
Offset 0x10 7390			*Auxiliary Capture Base Address*	
Offset 0x10 7394			*Auxiliary Capture Line Pitch*	
Miscellaneous Registers				
Offset 0x10 7800—79FC			*Coefficient Table #1 Taps 0-5 (Horizontal)*	

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VIDEO INPUT PROCESSOR (VIP) 2 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Interrupt & Status Control Registers				
Offset 0x10 7FE0			*Interrupt Status*	
Offset 0x10 7FE4			*Interrupt Enable*	
Offset 0x10 7FE8			*Interrupt Clear*	
Offset 0x10 7FEC			*Interrupt Set*	
Offset 0x10 7FF4			*POWERDOWN*	
Offset 0x10 7FFC			*Module ID*	

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SSI Port Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.12)

SSI PORT REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 8000			*SSI Control Register 1*	
31:11		-	Unused	
10	R/W	0	STORE_MP_LF	Set to store memory pointer to the beginning of a packet when that packet's last frame is received. Otherwise, the memory pointer is stored when the first frame of a packet is received.
9	R/W	0	EN_FR_ERR_INT	Set to enable the Frame-Error Interrupt.
8	R/W	0	EN_PI_ERR_INT	Set to enable the interrupt due to PI-Bus ERR during DMA.
7	R/W	0	EN_RX	Set to enable the receiver state machine. When cleared, inputs (FS, DIN) are ignored after the current frame is over.
6	R/W	0	EN_TX	Set to enable the transmit state machine. When cleared, DOUT is tri-stated at the end of the frame.
5		-	Unused	
4	R/W	0	RX_CH_RST	Receive channel reset. Same as a hard reset except that register settings are not changed. Inputs are ignored.
3	R/W	0	TX_CH_RST	Transmit channel reset. Same as a hard reset except that register settings are not changed. Outputs are tri-stated.
2	R/W	0	EN_GLO_INT	SSI Global Interrupt Enable. Set to 1 to enable interrupt from the SSI module.
1:0	R/W	00	EXT_DEVICE	Specify the external device 00 = PSB-4596 01 = STLC-7550 10 = Reserved 11 = Reserved
Offset 0x10 8004			*SSI Control Register 2*	
31	R/W	0	EN_RXDMA_OVN_INT_D	Set to enable Receive DMA Buffer 'D' Overrun Interrupt.
30	R/W	0	EN_RXDMA_OVN_INT_C	Set to enable Receive DMA Buffer 'C' Overrun Interrupt.
29	R/W	0	EN_RXDMA_OVN_INT_B	Set to enable Receive DMA Buffer 'B' Overrun Interrupt
28	R/W	0	EN_RXDMA_OVN_INT_A	Set to enable Receive DMA Buffer 'A' Overrun Interrupt.
27:24		-	Unused	
23	R/W	0	EN_RXBLK_INT	Set to enable the generation of interrupt when a data block of the size as specified in the Operating Block Size register has been received and stored in memory.
22	R/W	0	EN_RXDMA_FULL_INT_D	Set to enable Receive DMA Buffer 'D' Full Interrupt.
21	R/W	0	EN_RXDMA_FULL_INT_C	Set to enable Receive DMA Buffer 'C' Full Interrupt.

SSI PORT REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
20	R/W	0	EN_RXDMA_FULL_INT_B	Set to enable Receive DMA Buffer 'B' Full Interrupt.
19	R/W	0	EN_RXDMA_FULL_INT_A	Set to enable Receive DMA Buffer 'A' Full Interrupt.
18	R/W	0	EN_RXDMA_PPONG	Receive DMA Mode. Logic '1' to enable ping-pong DMA.
17	R/W	0	EN_RXDMA_AUTOINIT	Receive DMA Mode: Logic '0' for normal mode Logic '1' for auto-initialize mode
16	R/W	0	EN_RXDMA	Receive DMA enable.
15	R/W	0	EN_TXBLK_INT	Set to enable the generation of interrupt when a data block of the size as specified in the Operating Block Size register has been fetched from memory.
14	R/W	0	EN_TXDMA_UNR_INT_B	Set to enable Transmit DMA Buffer 'B' Underrun Interrupt.
13	R/W	0	EN_TXDMA_UNR_INT_A	Set to enable Transmit DMA Buffer 'A' Underrun Interrupt.
12	R/W	0	EN_TXDMA_EMP_INT_B	Set to enable Transmit DMA Buffer 'B' Empty Interrupt.
11	R/W	0	EN_TXDMA_EMP_INT_B	Set to enable Transmit DMA Buffer 'A' Empty Interrupt.
10	R/W	0	EN_TXDMA_PPONG	Transmit DMA Mode. Logic '1' to enable ping-pong DMA.
9	R/W	0	EN_TXDMA_AUTOINIT	Transmit DMA Mode: Logic '0' for normal mode Logic '1' for auto-initialize mode
8	R/W	0	EN_TXDMA	Transmit DMA enable.
7:6		-	Unused	
5	R/W	0	EN_RXWTM_INT_D	Enables the interrupt generated when Receive Buffer D reaches the watermark specified in register 0x054.
4	R/W	0	EN_RXWTM_INT_C	Enables the interrupt generated when Receive Buffer C reaches the watermark specified in register 0x054.
3	R/W	0	EN_RXWTM_INT_B	Enables the interrupt generated when Receive Buffer B reaches the watermark specified in register 0x050.
2	R/W	0	EN_RXWTM_INT_A	Enables the interrupt generated when Receive Buffer A reaches the watermark specified in register 0x050.
1	R/W	0	EN_CMD_SENT_COD_INT	Set to enable the interrupt generated when a command has been sent to the modem codec.
0	R/W	0	EN_RDATA_AVAIL_COD_INT	Interrupt Set to enable the interrupt generated when read data from the external modem codec is available.
Offset 0x10 8008			*SSI Status Register * Please see note below. **	
31	R/W	0	PI_ERR	Bus error: DMA transfers on PI-Bus terminated by ERR.
30	R/W	0	FRAME_ERR	No Frame Detected Error / Unexpected Frame Error.
29	R/W	0	RXDMA_OVRUN_ERR_D	Receive DMA Buffer 'D' overrun.
28	R/W	0	RXDMA_OVRUN_ERR_C	Receive DMA Buffer 'C' overrun.
27	R/W	0	RXDMA_OVRUN_ERR_B	Receive DMA Buffer 'B' overrun.
26	R/W	0	RXDMA_OVRUN_ERR_A	Receive DMA Buffer 'A' overrun.
25	R/W	0	TXDMA_OVRUN_ERR_B	Transmit DMA Buffer 'B' underrun.
24	R/W	0	TXDMA_OVRUN_ERR_A	Transmit DMA Buffer 'A' underrun.
23	R/W	0	CMD_SENT	Set when a command has been sent to the external modem codec.

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SSI PORT REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
22	R/W	0	CODEC_RDATA_AVAIL	Set when read data from external modem codec is available for read.
21:16		0	Unused	
15	R/W	0	RXBLK_DONE	Set when a block of data as specified in Operating Block Size Reg has been put in memory.
14:12		0	Unused	
11	R/W	0	RXDMA_FULL_D	Receive DMA Buffer 'D' Full. Set when the end of Rx D is reached.
10	R/W	0	RXDMA_FULL_C	Receive DMA Buffer 'C' Full. Set when the end of Rx C is reached.
9	R/W	0	RXDMA_FULL_B	Receive DMA Buffer 'B' Full. Set when the end of Rx B is reached.
8	R/W	0	RXDMA_FULL_A	Receive DMA Buffer 'A' Full. Set when the end of Rx A is reached.
7	R/W	0	TXBLK_DONE	Set when a block of data as specified in Operating Block Size Reg has been transmitted.
6		0	Unused	
5	R/W	0	RX_WMARK_D	Set when the Receive Buffer D reaches its watermark.
4	R/W	0	RX_WMARK_C	Set when the Receive Buffer C reaches its watermark.
3	R/W	0	RX_WMARK_B	Set when the Receive Buffer B reaches its watermark.
2	R/W	0	RX_WMARK_A	Set when the Receive Buffer A reaches its watermark.
1	R/W	0	TXDMA_EMPTY_B	Transmit DMA Buffer 'B' Empty. Set after the last data in Tx B is fetched.
0	R/W	0	TXDMA_EMPTY_A	Transmit DMA Buffer 'A' Empty. Set after the last data in Tx A is fetched.
Note: Bits in this register (0x008) are set to logic "1" when their associated event occurs. Writing "1" to a bit clears it. Writing "0" to a bit has no affect.				
Offset 0x10 800C			*Codec Control Register*	
31	R/W	0	EN_RXCLK_DIV2	When set, the internal receive clock is divided by 2. The clock edge that samples the frame synchronization pulse asserted will resync the receive clock divider to be the data capture edge. Data samples will be captured every other clock thereafter until the end of the valid slots in the frame.
30:27	R/W	0	FRAM_RATE	Control the divide ratio for the programmable frame rate divider used to generate the frame sync pulses. Valid values are 1 to 16 with 16 corresponding to "0000".
26:23	R/W	0	VALID_LOT_SIZE	Control the valid slot size starting from Slot 1. A value of 0 corresponds to 16 slots.
22	R/W	0	EN_SYNC_PULSE	Set if each packet requires a sync pulse (applied to modem codec).
21	R/W	0	FRAM_SYNC_POLARITY	Frame Sync Polarity controls which edge of the frame synchronization signal is active. Logic '0' indicates active rising edge. Logic '1' means falling edge.
20	R/W	0	TX_CLK_POLARITY	Transmit Clock Polarity. Data are transmitted on the rising edge of SCLK if TCP = '0'; on the falling edge of TCP = '1'.
19	R/W	0	RX_CLK_POLARITY	Receive Clock Polarity determines the sample clock's edge. Data are sampled on the falling edge of SCLK if RCP = '0'; on the rising edge if RCP = '1'.
18		-	Unused	

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SSI PORT REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
17	R/W	0	RX_SHIFT_LSB	Receive Shift Direction bit controls the shift direction of the receive shift register. Data is shifted in lsb first when RSD = ’1’ and msb first when RSD = ’0’.
16		-	Unused	
15:0	R/W	0	STLC7550 control bits[15:0] or PSB4596 control bits[7:0]	Refer to the data sheet of these ICs. In the case of the PSB4596, bits [15:8] are unused.
Offset 0x10 8010			*Codec Status Register*	
31:19		-	Unused	
18	R	0	SERIALIZER_EMPTY	Set when the last data bit has been shifted out of the serializer. It is cleared on writes to the Codec Status register.
17	R	0	CCR_SENT_TO_TX	Similar to Bit 23 of the SSI Status register but not dependent on the interrupt enable bit. It’s intended for polling i.e., it’s set as long as the condition remains true. Set when the content of the Codec Control register has been transferred to the transmitter (serializer) and the former is ready to accept new write data. It is reset on writes to Codec Control or Codec Status registers.
16	R	0	CODEC_RDATA_AVAIL	Similar to Bit 22 of the SSI Status register but not dependent on the interrupt enable bit. It’s intended for polling i.e., it’s set as long as the condition remains true. Set when read data from external modem codec is available for read. It is cleared on writes to the Codec Status register.
15:0	R	0	CARRY_CNTRL_DATA	Bits [15:0] carry control data. On reads, they reflect the values in the STLC-7550’s Control register or the PSB 4596’s last valid status byte (bits [7:0] only). Writes to this register are ignored.
Offset 0x10 8014			*Transmit DMA Address Register A*	
31:2	R/W	0	TXDMA_ADDR_A	Physical Base Address of the data to be transmitted. A DMA page (base address + transfer length) must not cross the 16-MB page boundary. When only one DMA buffer is needed, either register set A or B could be used.
1:0		-	Unused	
Offset 0x10 8018			*Transmit DMA Transfer Length Register A*	
31:14		-	Unused	
13:0	R/W	0	TXDMA_LENGTH_A	Transfer Length in 32-bit words
Offset 0x10 801C			*Transmit DMA Address Register B*	
31:2	R/W	0	TXDMA_ADDR_B	Physical Base Address of the data to be transmitted A DMA page (base address + transfer length) must not cross the 16-MB page boundary. When only one DMA buffer is needed, either register set A or B could be used.
1:0		-	Unused	
Offset 0x10 8020			*Transmit DMA Transfer Length Register B*	
31:14		-	Unused	
13:0	R/W	0	TXDMA_LENGTH_B	Transfer Length in 32-bit words
Offset 0x10 8024			*Transmit DMA Current Word Count*	
31:16		-	Unused	
15	R	0	TXDMA_ACTIVE_B	Set if the Transmit DMA Channel B is active.

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SSI PORT REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
14	R	0	TXDMA_ACTIVE_A	Set if the Transmit DMA Channel A is active.
13:0	R	0	NUM_WORDS_FETCHED	Represents the number of data words that have been fetched from memory.
Offset 0x10 8028			*Receive DMA Address Register A*	
31:2	R/W	0	RXDMA_ADDR_A	Physical Base Address of the memory region where receive data are to be stored. A DMA page (base address + transfer length) must not cross the 16-MB page boundary. When only one DMA buffer is needed, either register set A, B, C, or D can be used. When used in pairs as ping-pong buffers, A goes with B, C with D.
1:0		-	Unused	
Offset 0x10 802C			*Receive DMA Transfer Length Register A*	
31:14		-	Unused	
13:0	R/W	0	RXDMA_LENGTH_A	Transfer Length in Words
Offset 0x10 8030			*Receive DMA Address Register B*	
31:2	R/W	0	RXDMA_ADDR_B	Physical Base Address of the memory region where receive data are to be stored. A DMA page (base address + transfer length) must not cross the 16-MB page boundary. When only one DMA buffer is needed, either register set A, B, C, or D can be used. When used in pairs as ping-pong buffers, A goes with B, C with D.
1:0		-	Unused	
Offset 0x10 8034			*Receive DMA Transfer Length Register B*	
31:14		-	Unused	
13:0	R/W	0	RXDMA_LENGTH_B	Transfer Length in Words
Offset 0x10 8038			*Receive DMA Current Word Count for Channel A or B,*	
31:16		-	Unused	
15	R	0	RXDMA_ACTIVE_B	Set if the Receive DMA Channel B is active.
14	R	0	RXDMA_ACTIVE_A	Set if the Receive DMA Channel A is active.
13:0	R	0	NUM_WORDS_WRITTEN	Represents the number of data words moved to memory.
Offset 0x10 803C			*Receive DMA Address Register C*	
31:2	R/W	0	RXDMA_ADDR_C	Physical Base Address of the memory region where receive data are to be stored. A DMA page (base address + transfer length) must not cross the 16-MB page boundary. When only one DMA buffer is needed, either register set A, B, C, or D can be used. When used in pairs as ping-pong buffers, A goes with B, C with D.
1:0		-	Unused	
Offset 0x10 8040			*Receive DMA Transfer Length Register C*	
31:14		-	Unused	
13:0	R/W	0	RXDMA_LENGTH_C	Transfer Length in Words
Offset 0x10 8044			*Receive DMA Address Register D*	
31:2	R/W	0	RXDMA_ADDR_D	Physical Base Address of the memory region where receive data are to be stored. A DMA page (base address + transfer length) must not cross the 16-MB page boundary. When only one DMA buffer is needed, either register set A, B, C, or D can be used. When used in pairs as ping-pong buffers, A goes with B, C with D.
1:0		-	Unused	

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SSI PORT REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 8048			*Receive DMA Transfer Length Register D*	
31:14		-	Unused	
13:0	R/W	0	RXDMA_LENGTH_D	Transfer Length in Words
Offset 0x10 804C			*Receive DMA Current Word Count for Channel C or D*	
31:16		-	Unused	
15	R	0	RXDMA_ACTIVE_D	Set if the Receive DMA Channel D is active.
14	R	0	RXDMA_ACTIVE_C	Set if the Receive DMA Channel C is active.
13:0	R	0	NU_WORDS_WRITTEN	Represents the number of data words moved to memory.
Offset 0x10 8050			*Receive Buffer Watermark Register for Buffer A and/or B*	
31:16		-	Unused	
15:14	R/W	0	WATER_MARK_AB_SEL	00 = Watermark not applied. 01 = Watermark applied to Buffer A only. 10 = Watermark applied to Buffer B only. 11 = Watermark applied to both Buffers A and B.
13:0	R/W	0	WATER_MARK_AB_VALUE	Watermark Values. When the number of data words in buffers A and/ or B are equal to the number specified by Bits [13:0], an interrupt is generated. The Buffer Indicator Bits [15:14], determine to which buffer(s) this watermark is applied.
Offset 0x10 8054			*Receive Buffer Watermark Register for Buffer C and/or D*	
31:16		-	Unused	
15:14	R/W	0	WATER_MARK_CD_SEL	00 = Watermark not applied. 01 = Watermark applied to Buffer C only. 10 = Watermark applied to Buffer D only. 11 = Watermark applied to both Buffers A and B.
13:0	R/W	0	WATER_MARK_CD_VALUE	Watermark Values. When the number of data words in buffers A and/ or B are equal to the number specified by Bits [13:0], an interrupt is generated. The buffer Indicator, bits [15:14], determines to which buffer(s) this watermark is applied.
Offset 0x10 8058			*Operating Block Size Register*	
31:8		-	Unused	
7:0	R/W	0	OPER_BLK_SIZE	Operating Block Size specifies the number of data samples (in words) to be transferred to/from memory before an interrupt is generated. It's expected that the software DSP data pump processes transmit and receive data in blocks of the same sizes.
Offset 0x10 805C—8070			*Reserved*	
Offset 0x10 8074			*STLC Frame Width Register*	
31	R/W	0	SYNCDONE	SYNCDONE bit is set after software has figured out the correct sequence of sampled data and control data sent from the codec.
30	R/W	0	SWAP	SWAP bit is set to instruct the SSI hardware to reverse the current sequence of sampled data and control data being sent and received. This bit must be programmed to a proper value before or at the same time the SYNCDONE bit is set.
29:10		-	Unused	
9:0	R/W	0	TIME_INTERVAL_FS	Specify the time between frame synchronization pulses from the STLC-7550 in units of SCLKs. Used to detect missing-frame error.

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SSI PORT REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 8FF4			*Powerdown Register*	
31	R/W	0	POWER_DOWN	PD, SSI Powerdown indicator 1 = Powerdown (in this mode, no other registers are accessible). 0 = Power up.
30:0		-	Unused	
Offset 0x10 8FFC			*Module ID Register*	
31:16	R	0x010C	MODULE_ID	SSI Module ID number
15:12	R	0	REV_MAJOR	Major revision
11:8	R	0	REV_MINOR	Minor revision
7:0	R	0	APP_SIZE	Aperture size is 0 = 4 kB.

SPIDIF Output Port Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.23)

SPDIF OUTPUT PORT REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 9000			*SPDO_STATUS*	
Note: The clock frequency emitted by the DDS output can be found in Ch 6 Clock, Reset & Power Management registers at *Offset 0x04 711C DDS7_SPDO_CTL*				
31:5		-	Unused	
4	R/O	1	BUF1_ACTIVE	This flag gets set if the hardware is currently emitting DMA buffer 1 data and is negated when emitting DMA buffer 2 data.
3	R/O	0	UNDERRUN	This flag gets set if both DMA buffers were emptied before a new full buffer was assigned by software. The hardware has performed a normal buffer switch over and is emitting old data. IT can only be cleared by software write to ACK_UDR.
2	R/O	0	HBE (Bandwidth error)	Bandwidth Error. This flag gets set if the internal buffers in SPDO were emptied before new memory data was brought in. This flag can be cleared only by a software write to ACK_HBE.
1	R/O	0	BUF2_EMPTY	This flag gets set if DMA buffer 2 has been emptied by the SPDO hardware. The flag can be cleared only by a software write to ACK_BUF2.
0	R/O	0	BUF1_EMPTY	This flag gets set if DMA buffer 1 has been emptied by the SPDO hardware. The flag can be cleared only by a software write to ACK_BUF1.
Offset 0x10 9004			*SPDO_CTL*	
31	R/W	0	RESET	1 = Software Reset. Immediately resets the SPDO block. This should be used with extreme caution. Any ongoing transmission will be interrupted and receivers may be left in a strange state.
30	R/W	0	TRANS_ENABLE	1 = Enables transmission per the selected mode. 0 = Transmission Disabled. Stops any ongoing transmission after completing any actions related to the current data descriptor word.

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SPDIF OUTPUT PORT REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
29:27	R/W	000	TRANS_MODE	Transmission mode. 000 = IEC-60958 mode. Hardware performs bi-phase mark encoding, preamble and parity generation, and transmits one IEC-60958 subframe for each data descriptor word. 010 = Transparent mode, lsb first. The 32-bit data descriptor words are transmitted as is, lsb first. 011 = Transparent mode, msb first. The 32-bit data descriptor words are transmitted as is, msb first. Other codes are reserved for future extensions. Note: The transmission mode should only be changed while transmission is disabled.
26:8		-	Unused	
7	R/W	0	UDR_INTEN	If UDR_INTEN = 1 and UNDERRUN = 1, an interrupt is asserted to the chip level interrupt controller.
6	R/W	0	HBE_INTEN	If HBE_INTEN = 1 and HBE = 1, an interrupt is asserted to the chip level interrupt controller.
5	R/W	0	BUF2_INTEN	If BUF2_INTEN = 1 and BUF2_EMPTY = 1, an interrupt is asserted to the chip level interrupt controller.
4	R/W	0	BUF1_INTEN	If BUF1_INTEN = 1 and BUF1_EMPTY = 1, an interrupt is asserted to the chip level interrupt controller.
3	R/W	0	ACK_UDR	1 = Clear UNDERRUN. 0 = No effect. Always reads as 0.
2	R/W	0	ACK_HBE	1 = Clear HBE. 0 = No effect. Always reads as 0.
1	R/W	0	ACK_BUF2	1 = Clear BUF2_EMPTY. Informs SPDO that DMA buffer 2 is full. 0 = No effect. Always reads as 0.
0	R/W	0	ACK_BUF1	1 = Clear BUF1_EMPTY. Informs SPDO that DMA buffer 1 is full. 0 = No effect. Always reads as 0.
Offset 0x10 9008			*Reserved*	
31:0	R	0x0	Reserved	Legacy register. Always reads as ‘0’.
Offset 0x10 900C			*SPDO_BASE1*	
31:6	R/W	0x0	BASE1	SPDO_BASE1 contains the memory address of DMA buffer 1.
5:0	R	0x0	Reserved	Always reads as ‘0’.
Offset 0x10 90010			*SPDO_BASE2*	
31:6	R/W	0x0	BASE2	SPDO_BASE2 contains the memory address of DMA buffer 2.
5:0	R	0x0	Reserved	Always reads as ‘0’.
Offset 0x10 9014			*SPDO_SIZE*	
31:6	R/W	0x0	SIZE	SPDO_SIZE determines the size, in bytes, of both DMA buffers.
5:0	R	0x0	Reserved	Always reads as ‘0’.
Offset 0x10 9018—9FF0			*Reserved*	

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SPDIF OUTPUT PORT REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x10 9FF4			*SPDO_PWR_DWN*	
31:1		-	Unused	
0	R/W	0	PWR_DWN	Used to provide power control status for system software block power management.
Offset 0x10 9FFC			*SPDO_MODULE_ID*	
31:16	R/O	0x0121	ID	Module ID. This field identifies the block as type SPDO.
15:12	R/O	0	MAJ_REV	Major Revision ID
11:8	R/O	0	MIN_REV	Minor Revision ID
7:0	R/O	0	APERTURE	Aperture size. Identifies the MMIO aperture size in units of 4 kB for the SPDO block. SPDO has an MMIO aperture size of 4 kB. Aperture = 0, 4 kB.

SPIDIF Input Port Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.22)

SPDIF INPUT PORT REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x10 A000			*SPDI_CTL*	
31:9		-	Unused	
11:8	R/W	0	GL_FILTER	Input glitch filter control. These bits control the rejection of a glitch on the SPDI interface. 0000 = The Glitch Rejection Filter is disabled. 0001...1111 = An incoming signal transition must remain stable for (programmed value + 1) rising edges of OSC_CLK, otherwise it is rejected as a glitch.
7	R/W	0	UCBITS_SEL	User/Channel status bits select. Selects the set of subframes from which the user and channel status bits are extracted and written to the SPDI_UBITSx and SPDI_CBITSx registers. This bit is activated only on a block boundary, meaning that the bit can be changed at any time via software, but the update of the SPDI_UBITSx and SPDI_CBITSx registers with the new information will wait until a complete block has been received at the SPDIF input. 0 = subframe 1 is selected, user and channel status bits are extracted/written to UBITSx and CBITSx registers. 1 = subframe 2 is selected. User and channel status bits are extracted/written to UBITSx and CBITSx registers.
6:5	R/W	0	CHAN_MODE[1:0]	00 = Capture stereo left/right sample pairs (Default). 01 = Capture mono primary (subframe 1) channel. 10 = Capture mono secondary (subframe 2) channel. 11 = Reserved Note: The channel mode should only be changed while capture is disabled (i.e. CAP_ENABLE = 0).

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SPDIF INPUT PORT REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
4:3	R/W	0	SAMP_MODE[1:0]	**00 = 16-bit mode**. Subframe bits [27:12] inclusive are selected and stored. Hardware stores a single 16-bit word per subframe. If audio samples are actually larger than 16 bits, the most significant 16 bits of the audio sample will be selected and stored. **01= 32-bit mode**. Subframe bits [27:4] inclusive are selected and stored subject to SMASK. A 32-bit word is formed by bitwise masking the sample (subject to the value of SPDI_SMPMASK.SMASK) and padding '0' bits to the least significant end of the 24 bits. The resultant 32-bit words are of the form: 0xnnnnmm00 where the *n*s are the 16 subframe bits [27:12] and the *m*s are the eight masked subframe bits [11:4]. This provides for any audio sample size from 17 to 24 bits. (See the SPDI_SMPMASK register description for operation of the SMASK feature). SMASK only applies for this sample mode. **10 = Raw capture mode**. The entire subframe is captured and stored. The bi-phase portion of the subframe (i.e., bits [31:4]) are decoded into binary. Bits [3:0] are replaced with a code. The entire 32 bits are then stored as one unit. 11 = Reserved Note: The sample mode should only be changed while capture is disabled (i.e., CAP_ENABLE = '0').
2	R/W	0	DIAG_MODE	Diagnostic loopback mode. Used to diagnose the SPDIF IN block. 0 = The SPDIF IN input source is set to the SPDIF input pin (default). 1 = The SPDIF IN input source is set to the SPDIF OUT pin.
1	R/W	0	CAP_ENABLE	Writing a '1' to this bit enables capture per the selected mode. Writing a '0' here stops any ongoing capture after completing any actions related to the current audio sample.
0	R/W	0	RESET	Writing a '1' to this bit resets the SPDI block. The registers of the SPDI will all be reset to '0s'. This should be used with caution. Any ongoing capture will be interrupted.
Offset 0x10 A004			*SPDI_BASE1*	
31:6	R/W	0	BASE1	Selects the main memory buffer starting addresses used for DMA of audio data samples. Note: Any change to the SPDI_BASE1 register should only be done while a memory buffer is not being used by the hardware DMA.
5:0	R	0	Reserved	
Offset 0x10 A008			*SPDI_BASE2*	
31:6	R/W	0	BASE2	Selects the main memory buffer starting addresses used for DMA of audio data samples. Note: Any change to the SPDI_BASE2 register should only be done while a memory buffer is not being used by the hardware DMA.
5:0	R	0	Reserved	Hardwired to logic '0'
Offset 0x10 A00C			*SPDI_SIZE*	
31:6	R/W	0	SIZE (in bytes)	The size of the DMA buffers is specified in the SPDI_SIZE register. Note hardware limits the buffer size and starting address to be aligned to 64-byte addresses. Assignment to SPDI_BASE1, SPDI_BASE2 and SPDI_SIZE have no effect on the state of the SPDI_STATUS flags.
5:0	R	0	Reserved	Hardwired to logic '0'

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SPDIF INPUT PORT REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 A010			*SPDI_BPTR*	
31:0	R	0	ADDRESS	To aid software with finding the start of a block in memory, the SPDI_BPTR contains the address of the first occurrence of a frame 0 (indicating the starting boundary of a complete 192-frame block) within the currently filling memory buffer: BUF1 or BUF2. This is useful during capture of non-PCM coded data found in IEC61937 data streams.
Offset 0x10 A014			*SPDI_SMPMASK*	
31:8		-	Unused	
7:0	R/W	0x00	SMASK	Allows per bit masking the least significant 8 bits of the incoming samples (corresponding to subframe bits [11:4]). The SMASK setting only applies to 32-bit capture mode (i.e., SAMP_MODE = 01). The 8 bits of SMASK will determine which subframe bits [11:4] will be captured and stored in memory. Note: Setting SMASK[7:0] bits to logic '1' will zero the corresponding subframe bit [11:4]. Others will pass unchanged.
Offset 0x10 A018			*SPDI_CBITS1*	
31:0	R	0	CBITS [31:0]	Channel Status register 1 contains bytes 0, 1, 2 and 3 of the current Channel Status block according to SPDI_CTL.UCBITS_SEL. It will always reflect the condition of the current decoded block of 192 frames and will always start at the block boundary. Register bit meaning will depend upon the source transmission (i.e., consumer vs. professional).
Offset 0x10 A01C			*SPDI_CBITS2*	
31:0	R	0	CBITS [31:0]	Channel Status register 2 contains bytes 4, 5, 6 and 7 of the current Channel Status block according to SPDI_CTL.UCBITS_SEL.
Offset 0x10 A020			*SPDI_CBITS3*	
31:0	R	0	CBITS [31:0]	Channel Status register 3 contains bytes 8, 9,10 and 11 of the current Channel Status block according to SPDI_CTL.UCBITS_SEL.
Offset 0x10 A024			*SPDI_CBITS4*	
31:0	R	0	CBITS [31:0]	Channel Status register 4 contains bytes 12, 13, 14 and 15 of the current Channel Status block according to SPDI_CTL.UCBITS_SEL.
Offset 0x10 A028			*SPDI_CBITS5*	
31:0	R	0	CBITS [31:0]	Channel Status register 5 contains bytes 16,17,18 and 19 of the current Channel Status block according to SPDI_CTL.UCBITS_SEL.
Offset 0x10 A02C			*SPDI_CBITS6*	
31:0	R	0	CBITS [191:159]	Channel Status register 6 contains bytes 20, 21, 22 and 23 of the current Channel Status block according to SPDI_CTL.UCBITS_SEL.
Offset 0x10 A030			*SPDI_UBITS1*	
31:0	R	0	UBITS [31:0]	User bit 1 contains the state of user bytes 0,1, 2 and 3 of the block according to SPDI_CTL.UCBITS_SEL. The SPDI_UBITS register will always reflect the condition of the current decoded block of 192 frames. Register bit meaning will depend upon the source transmission.

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SPDIF INPUT PORT REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 A034			*SPDI_UBITS2*	
31:0	R	0	UBITS [31:0]	User bit 2 contains the state of user bytes 4, 5, 6 and 7 of the block according to SPDI_CTL.UCBITS_SEL. The SPDI_UBITS register will always reflect the condition of the current decoded block of 192 frames. Register bit meaning will depend upon the source transmission.
Offset 0x10 A038			*SPDI_UBITS3*	
31:0	R	0	UBITS [31:0]	User bit 3 contains the state of user bytes 8, 9, 10 and 11 of the block according to SPDI_CTL.UCBITS_SEL. The SPDI_UBITS register will always reflect the condition of the current decoded block of 192 frames. Register bit meaning will depend upon the source transmission.
Offset 0x10 A03C			*SPDI_UBITS4*	
31:0	R	0	UBITS [31:0]	User bit 4 contains the state of user bytes 12, 13, 14 and 15 of the block according to SPDI_CTL.UCBITS_SEL. The SPDI_UBITS register will always reflect the condition of the current decoded block of 192 frames. Register bit meaning will depend upon the source transmission.
Offset 0x10 A040			*SPDI_UBITS5*	
31:0	R	0	UBITS [31:0]	User bit 5 contains the state of user bytes 16, 17, 18 and 19 of the block according to SPDI_CTL.UCBITS_SEL. The SPDI_UBITS register will always reflect the condition of the current decoded block of 192 frames. Register bit meaning will depend upon the source transmission.
Offset 0x10 A044			*SPDI_UBITS6*	
31:0	R	0	UBITS [191:159]	User bit 6 contains the state of user bytes 20, 21, 22 and 23 of the block according to SPDI_CTL.UCBITS_SEL. The SPDI_UBITS register will always reflect the condition of the current decoded block of 192 frames. Register bit meaning will depend upon the source transmission.
Offset 0x10 A048—AFDC			*Reserved*	

SPDIF INPUT PORT REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 AFE0			*SPDI_STATUS*	
31:10		-	Unused	
9	R	0	UNLOCK	UNLOCK active. This flag gets set to logic '1' if the SPDIF receiver is NOT locked onto an incoming stream. Programmers can use this UNLOCK indication, in conjunction with the LOCK bit, to determine the state of the receiver or to make a decision to adjust the oversampling frequency. See the definition of the LOCK bit. Possible causes of an out-of-lock state are: i) The oversampling frequency is too high or too low with respect to the applied input SPDIF sample rate. ii) Too much jitter in SPDIF input stream. iii) Absent, invalid or corrupted SPDIF stream applied to the interface/receiver. The flag can be cleared by a software write to UNLOCK_CLR.

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SPDIF INPUT PORT REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
8	R	0	UCBITS	User/Channel bits available. This flag gets set if a new set of user data bits and channel status bits have been written to the SPDI_UBITSx and SPDI_CBITSx registers. Updated on a block basis.
7	R	0	LOCK	LOCK active. 1 = The SPDIF receiver achieved lock onto the incoming stream. Use this LOCK flag, in conjunction with the UNLOCK flag, to determine the state of the receiver or to make a decision to adjust the oversampling frequency. The flag can be cleared by a software write to LOCK_CLR. Note: A valid sequence of preambles is not required for LOCK.
6	R	0	VERR	Validity Error. 1 = The hardware encounters a subframe that has the validity flag set to 1, indicating that the payload portion of the subframe is not reliable. The flag can be cleared by a software write to VERR_CLR.
5	R	0	PERR	Parity Error. 1 = The hardware encounters a subframe that has a parity error. Parity is even for the subframe and applies to subframe bits [31:4] inclusive. Normally, the external SPDIF transmitter will set the subframe P bit to logic ‘1’ or logic ‘0’ so that bits [31:4] have an even number of logic “1s” and “0s”. The flag can be cleared by a software write to PERR_CLR.
4	R	0	OVERRUN	1 = Both external main memory DMA buffers are filled before a new empty buffer is assigned by the system control CPU. Hardware has performed a normal buffer switch over and is overwriting fresh, unconsumed data. This flag can be cleared by software write to OVR_CLR.
3	R	0	HBE (Bandwidth error)	Bandwidth Error. 1 = The internal hardware DMA buffers in SPDI are full and at least one of them was not emptied before new input data arrived on the SPDI interface, indicating that DMA service latency is too long. This flag can be cleared by a software write to HBE_CLR.
2	R	0	BUF1_ACTIVE	This flag gets set to logic ‘1’ if the hardware is currently filling memory DMA buffer 1. Otherwise, it is reset to logic ‘0’. This flag can be cleared by a software write to BUF1_ACTIVE_CLR.
1	R	0	BUF2_FULL	This flag gets set to logic ‘1’ if memory DMA buffer 2 has been filled by the SPDI hardware. It can be cleared by a software write to BUF2_FULL_CLR.
0	R	0	BUF1_FULL	This flag gets set to logic ‘1’ if memory DMA buffer 1 has been filled by the SPDI hardware. It can be cleared by a software write to BUF1_FULL_CLR.
Offset 0x10 AFE4			*SPDI_INTEN*	
31:10		-	Unused	
9	R/W	0	UNLOCK_ENBL	1 = UNLOCK bit in SPDI_STATUS is enabled for interrupts. 0 = UNLOCK bit in SPDI_STATUS is disabled for interrupts.
8	R/W	0	UCBITS_ENBL	1 = UCBITS bit in SPDI_STATUS is enabled for interrupts. 0 = UCBITS bit in SPDI_STATUS is disabled for interrupts.
7	R/W	0	LOCK_ENBL	1 = LOCK bit in SPDI_STATUS is enabled for interrupts. 0 = LOCK bit in SPDI_STATUS is disabled for interrupts.
6	R/W	0	VERR_ENBL	1 = VERR bit in SPDI_STATUS is enabled for interrupts. 0 = VERR bit in SPDI_STATUS is disabled for interrupts.

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SPDIF INPUT PORT REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
5	R/W	0	PERR_ENBL	1 = PERR bit in SPDI_STATUS is enabled for interrupts. 0 = PERR bit in SPDI_STATUS is disabled for interrupts.
4	R/W	0	OVR_ENBL	1 = OVERRUN bit in SPDI_STATUS is enabled for interrupts. 0 = OVERRUN bit in SPDI_STATUS is disabled for interrupts.
3	R/W	0	HBE_ENBL	1 = HBE bit in SPDI_STATUS is enabled for interrupts. 0 = HBE bit in SPDI_STATUS is disabled for interrupts.
2	R/W	0	BUF1_ACTIVE_ENBL	1 = BUF1_ACTIVE bit in SPDI_STATUS is enabled for interrupts. 0 = BUF1_ACTIVE bit in SPDI_STATUS is disabled for interrupts.
1	R/W	0	BUF2_FULL_ENBL	1 = BUF2_FULL bit in SPDI_STATUS is enabled for interrupts. 0 = BUF2_FULL bit in SPDI_STATUS is disabled for interrupts.
0	R/W	0	BUF1_FULL_ENBL	1 = BUF1_FULL bit in SPDI_STATUS is enabled for interrupts. 0 = BUF1_FULL bit in SPDI_STATUS is disabled for interrupts.
Offset 0x10 AFE8			*SPDI_INTCLR*	
31:10		-	Unused	
9	R/W	0	UNLOCK_CLR	1 = Clear UNLOCK bit in SPDI_STATUS. 0 = No effect
8	W	0	UCBITS_CLR	1 = Clear UCBITS in SPDI_STATUS. 0 = No effect.
7	W	0	LOCK_CLR	1 = Clears LOCK in SPDI_STATUS. 0 = No effect.
6	W	0	VERR_CLR	1 = Clear VERR in SPDI_STATUS. 0 = No effect
5	W	0	PERR_CLR	1 = Clear PERR in SPDI_STATUS. 0 = No effect.
4	W	0	OVR_CLR	1 = Clear OVERRUN in SPDI_STATUS. 0 = No effect.
3	W	0	HBE_CLR	1 = Clear HBE in SPDI_STATUS. 0 = No effect.
2	W	0	BUF1_ACTIVE_CLR	1 = Clear BUF1_ACTIVE in SPDI_STATUS. 0 = No effect.
1	W	0	BUF2_FULL_CLR	1 = Clear BUF2_FULL in SPDI_STATUS. 0 = No effect.
0	W	0	BUF1_FULL_CLR	1 = Clear BUF1_FULL in SPDI_STATUS. 0 = No effect.
Offset 0x10 AFEC			*SPDI_INTSET*	
31:10		-	Unused	
9	W	0	UNLOCK_SET	1 = UNLOCK bit in SPDI_STATUS is to be set to logic ‘1’. Level trigger interrupt will be raised to the external interrupt controller if the corresponding enable bit is set to logic ‘1’. 0 = No effect
8	W	0	UCBITS_SET	1 = UCBITS bit in SPDI_STATUS is to be set to logic ‘1’. Level trigger interrupt will be raised to the external interrupt controller if the corresponding enable bit is set to logic ‘1’. 0 = No effect

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SPDIF INPUT PORT REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
7	W	0	LOCK_SET	1 = LOCK bit in SPDI_STATUS is to be set to logic ‘1’. Level trigger interrupt will be raised to the external interrupt controller if the corresponding enable bit is set to logic ‘1’. 0 = No effect
6	W	0	VERR_SET	1 = VERR bit in SPDI_STATUS is to be set to logic ‘1’. Level trigger interrupt will be raised to the external interrupt controller if the corresponding enable bit is set to logic ‘1’. 0 = No effect
5	W	0	PERR_SET	1 = PERR bit in SPDI_STATUS is to be set to logic ‘1’. Level trigger interrupt will be raised to the external interrupt controller if the corresponding enable bit is set to logic ‘1’. 0 = No effect
4	W	0	OVR_SET	1 = OVERRUN bit in SPDI_STATUS is to be set to logic ‘1’. Level trigger interrupt will be raised to the external interrupt controller if the corresponding enable bit is set to logic ‘1’. 0 = No effect
3	W	0	HBE_SET	1 = HBE bit in SPDI_STATUS is to be set to logic ‘1’. Level trigger interrupt will be raised to the external interrupt controller if the corresponding enable bit is set to logic ‘1’. 0 = No effect
2	W	0	BUF1_ACTIVE_SET	1 = BUF1_ACTIVE bit in SPDI_STATUS is to be set to logic ‘1’. Level trigger interrupt will be raised to the external interrupt controller if the corresponding enable bit is set to logic ‘1’. 0 = No effect
1	W	0	BUF2_FULL_SET	1 = BUF2_FULL bit in SPDI_STATUS is to be set to logic ‘1’. Level trigger interrupt will be raised to the external interrupt controller if the corresponding enable bit is set to logic ‘1’. 0 = No effect
0	W	0	BUF1_FULL_SET	1 = BUF1_FULL bit in SPDI_STATUS is to be set to logic ‘1’. Level trigger interrupt will be raised to the external interrupt controller if the corresponding enable bit is set to logic ‘1’. 0 = No effect

SPDIF INPUT PORT REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x10 AFF4			*SPDI_PWR_DWN*	
31:1		-	Unused	
0	R/W	0	PWR_DWN	The bit is used to provide power control status for system software block power management.
Offset 0x10 AFFC			*SPDI_MODULE_ID*	
31:16	R	0x0110	Module ID	This field identifies the block as type SPDIF IN. SPDIF IN ID = 0x0110
15:12	R	0	MAJ_REV	Major Revision ID
11:8	R	0	MIN_REV	Minor Revision ID
7:0	R	0	APERTURE	Aperture size

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MBS Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.27)

MEMORY BASED SCALER (MBS) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Operating Mode Control Registers				
Offset 0x10 C000			*MBS Mode Control*	
31:30	R/W	0	DPM_SEQ	Data path sequence 0x = Bypass all filter stages (format conversion only). 10 = HSP -> VSP 11 = VSP -> HSP
29:26		-	Unused	
25:24	R/W	0	VSP_DEINTERLACE	De-interlacing mode 00 = No de-interlacing 01 = Vertical temporal median 10 = Majority selection algorithm (2 field) 11 = Majority selection algorithm (3 field) (Note: 3-field MS function is not implemented.)
23:22		-	Unused	
21:20	R/W	0	COEFF_LUT_MODE	Coefficient look-up table access mode 00 = Each table gets written separately. 01 = Writes to coefficient table 2 are copied into table 3. 10 = Writes to coefficient table 1 are copied into table 2. 11 = Writes to coefficient table 1 are copied into tables 2 and 3.
19		-	Unused	
18	R/W	0	NO_AUTO_SKIP	Disable Auto Skip When set to zero (default) the MBS will automatically skip all remaining operations within a task once the TASK_DONE interrupt was generated. If enable the MBS will continue until all pipeline stages are idle.
17	W	0	SKIP_TASK	Skip current task. Writing a one into this bit will reset the current task and continue with previously scheduled tasks.
16	W	0	SOFT_RESET	Soft reset Writing a one into this bit will reset the block and all outstanding scaling tasks.
15		-	Unused	
14	R/W	0	IFF_CLAMP	Clamp mode for IFF (affects U/V only). 0 = Clamp from 0-255. 1 = Clamp from 16 - 240 (CCIR range.
13:12	R/W	0	IFF_MODE	Interpolation mode 00 = Bypass 01 = Reserved 10 = Co-sited 11 = Interspersed
11		-	Unused	
10	R/W	0	DFF_CLAMP	Clamp mode for DFF (affects U/V only) 0 = Clamp from 0-255. 1 = Clamp from 16 - 240 (CCIR range).
9:8	R/W	0	DFF_MODE	Decimation mode 00 = Bypass 01 = Co-sited (subsample) 10 = Co-sited (lowpass) 11 = Interspersed

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MEMORY BASED SCALER (MBS) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
7	R/W	0	VSP_CLAMP	Clamp mode for VSP 0 = Clamp from 0-255. 1 = Clamp to CCIR range defined by VSP_RGB (bit 6.)
6	R/W	0	VSP_RGB	Color space mode, defines CCIR clamping range for VSP 0 = Processing in YUV color space (CCIR range: 16 - 235(Y), 16 - 240(U/V)) 1 = Processing in RGB color space (CCIR range: 16 - 235)
5:4	R/W	0	VSP_MODE	Vertical processing mode 00 = Bypass mode 01 = Reserved 10 = Normal polyphase mode 11 = Reserved
3	R/W	0	HSP_CLAMP	Clamp mode for HSP 0 = Clamp from 0-255. 1 = Clamp to CCIR range defined by HSP_RGB (bit 2).
2	R/W	0	HSP_RGB	Color space mode, defines CCIR clamping range for HSP 0 = Processing in YUV color space (CCIR range: 16 - 235(Y), 16 - 240(U/V)) 1 = Processing in RGB color space (CCIR range: 16 - 235)
1:0		0	HSP_MODE	Horizontal processing mode 00 = Bypass mode 01 = Color space matrix mode 10 = Normal polyphase mode 11 = Transposed polyphase mode

MEMORY BASED SCALER (MBS) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Video Information Registers				
Offset 0x10 C040			*Task FIFO*	
31:3	W	0	TASK_BASE	Scale task FIFO Must be aligned to 8-byte boundary.
2		-	Unused	
1:0	W	0	TASK_CMD	Command mode 00 = Process task descriptor at given base. 01 = Start scaling with current register settings. 10 = Start and queue next. 11 = Reserved
Offset 0x10 C044			*Task Status*	
31:4		-	Unused	
3:0	R	0	TASK_PENDING	Number of pending scaling tasks (including current)

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MEMORY BASED SCALER (MBS) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Input Format Control Registers				
Offset 0x10 C100			*Input Format*	
31:30	R/W	0	PFU_BAMODE	Base address mode 00 = Single set (e.g., progressive video source) base 1-3 according to number of planes (plane 1-3) 01 = Alternate sets each line (e.g., interlaced video source) base 1-3, first line in, etc. (plane 1-3) base 4-6, second line in, etc. (plane 1-3) 1x = Reserved
29:16		-	Unused	
15	R/W	0	PFU_HFLIP	Mirror input mode 0 = Normal 1 = Mirrored input
14	R/W	0	PFU_AMI	Alternate memory interleaving format 0 = Default memory interleaving 1 = Memory interleaving used by MPEG block
13	R/W	0	PFU_ENDIAN	Input format Endianness 0 = Same as system Endianness 1 = Opposite of system Endianness
12:8		-	Unused	
7:0	R/W	0	PFU_IPFMT	Input formats 00 (hex) = YUV 4:2:0, semi-planar 03 (hex) = YUV 4:2:0, planar 08 (hex) = YUV 4:2:2, semi-planar 0B (hex) = YUV 4:2:2, planar 0F (hex) = RGB or YUV 4:4:4, planar 24 (hex) = 1-bit indexed 45 (hex) = 2-bit indexed 66 (hex) = 4-bit indexed 87 (hex) = 8-bit indexed A0 (hex) = Packed YUY2 4:2:2 A1 (hex) = Packed UYVY 4:2:2 AC (hex) = 16-bit variable contents 4:4:4 E8 (hex) = 32-bit variable contents 4:2:2 EC (hex) = 32-bit variable contents 4:4:4
Offset 0x10 C104			*Source Window Size*	
31:27		-	Unused	
26:16	R/W	0	PFU_LSIZE	Line size Defines size of input window. 1 = One pixel
15:11		-	Unused	
10:0	R/W	0	PFU_LCOUNT	Line count Defines size of input window. 1 = One line
Offset 0x10 C108			*Variable Format Register*	
31:29	R/W	0	PFU_SIZE_C4 [2:0]	Size component #4 (alpha or V) Number of bits minus 1 (e.g., 7 = 8 bits per component)
28:24	R/W	0	PFU_OFFS_C4 [4:0]	Offset component #4 (alpha or V) Index of MSB position within 32-bit word (0-31)

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MEMORY BASED SCALER (MBS) REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
23:21	R/W	0	PFU_SIZE_C3 [2:0]	Size component #3 (V or B or Y2) number of bits minus 1 (e.g., 7 = 8 bits per component)
20:16	R/W	0	PFU_OFFS_C3 [4:0]	Offset component #3 (V or B or Y2) index of MSB position within 32-bit word (0-31)
15:13	R/W	0	PFU_SIZE_C2[2:0]	Size component #2 (U or G) number of bits minus 1 (e.g., 7 = 8 bits per component)
12:8	R/W	0	PFU_OFFS_C2[4:0]	Offset component #2 (U or G) index of MSB position within 32-bit word (0-31)
7:5	R/W	0	PFU_SIZE_C1[2:0]	Size component #1 (Y or R) number of bits minus 1 (e.g., 7 = 8 bits per component)
4:0	R/W	0	PFU_OFFS_C1[4:0]	Offset component #1 (Y or R) index of MSB position within 32-bit word (0-31)

MEMORY BASED SCALER (MBS) REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Video Input Address Generation Control Registers				
Offset 0x10 C140			*Source Base Address #1*	
31:26		-	Unused	
25:3	R/W	0	PFU_BASE1	Base address DMA #1, used depending on PFU_BAMODE setting.
2:0	R/W	0	PFU_OFFSET1	Base address byte offset DMA #1. Bits define pixel offset within multi pixel 64-bit words (e.g., a 16-bit pixel can be placed on any 16-bit boundary).
Offset 0x10 C144			*Source Line Pitch #1*	
31:15		-	Unused	
14:3	R/W	0	PFU_PITCH1	Line pitch DMA #1, signed value (two's complement) is used for all packed formats and for plane 1.
2:0		-	Unused	
Offset 0x10 C148			*Source Base Address #2*	
31:26		-	Unused	
25:3	R/W	0	PFU_BASE2	Base address DMA #2, used depending on PFU_BAMODE setting.
2:0	R/W	0	PFU_OFFSET2	Base address byte offset DMA #2. Bits define pixel offset within multi pixel 64-bit words (e.g., a 16-bit pixel can be placed on any 16-bit boundary).
Offset 0x10 C14C			*Source Line Pitch #2*	
31:15		-	Unused	
14:3	R/W	0	PFU_PITCH2	Line pitch DMA #2, signed value (two's complement) is used for planes 2 and 3.
2:0		-	Unused	
Offset 0x10 C150			*Source Base Address #3*	
31:26		-	Unused	
25:3	R/W	0	PFU_BASE3	Base address DMA #3, used depending on PFU_BAMODE setting.

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MEMORY BASED SCALER (MBS) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
2:0	R/W	0	PFU_OFFSET3	Base address byte offset DMA #3. Bits define pixel offset within multi pixel 64-bit words (e.g., a 16-bit pixel can be placed on any 16-bit boundary).
Offset 0x10 C154			*Source Base Address #4*	
31:26		-	Unused	
25:3	R/W	0	PFU_BASE4	Base address DMA #4, used depending on PFU_BAMODE setting.
2:0		-	Unused	
Offset 0x10 C158			*Source Base Address #5*	
31:26		-	Unused	
25:3	R/W	0	PFU_BASE5	Base address DMA #5, used depending on PFU_BAMODE setting.
2:0		-	Unused	
Offset 0x10 C15C			*Source Base Address #6*	
31:26		-	Unused	
25:3	R/W	0	PFU_BASE6	Base address DMA #6, used depending on PFU_BAMODE setting.

MEMORY BASED SCALER (MBS) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Horizontal Video Processing Control Registers				
Offset 0x10 C200			*Initial Zoom*	
31:29	R/W	0	HSP_PHASE_MODE[2:0]	Phase mode 0 = 64 phases 1 = 32 phases 2 = 16 phases 3 = 8 phases 4 = 4 phases 5 = 2 phases 6 = Fixed phase 7 = Linear phase interpolation (only valid for 4 component mode)
28	R/W	0	HSP_NO_CROP	Disable line length cropping. 0 = Cropping enabled (default). 1 = Cropping disabled, used for striped scaling tasks.
27		-	Unused	
26	R/W	0	HSP_FIR_COMP[1:0]	Horizontal filter components 0 = Three components, 6-tap FIR each 1 = Four components, 3-tap FIR each In color space matrix mode this value has to remain zero.
25:20		-	Unused	
19:0	R/W	0	HSP_ZOOM_0[19:0]	Initial zoom for 1st pixel in line (unsigned, lsb = 2^{-16}) 2 0000 (hex) = Downscale 50% 1 0000 (hex) = No scaling = 100% 0 8000 (hex) = Zoom 2 x (transposed: downscale 50%) Values above 10000 (hex) are not valid in transposed mode.
Offset 0x10 C204			*Phase Control*	

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MEMORY BASED SCALER (MBS) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
31		-	Unused	
30:28	R/W	0	HSP_QSHIFT[2:0]	Quantization shift control is used to change quantization before being multiplied with HSP_MULTIPLY. 100 (bin) = Divide by 16. 101 (bin) = Divide by 8. 110 (bin) = Divide by 4. 111 (bin) = Divide by 2. 000 (bin) = Multiply by 1. 001 (bin) = Multiply by 2. 010 (bin) = Multiply by 4. 011 (bin) = Multiply by 8. Warning: A value range overflow caused by an improper quantization shift can not be compensated later by multiplying with a HSP_MULTIPLY value below 0.5.
27:26		-	Unused	
25	R/W	0	HSP_QSIGN	Quantization sign bit
24:16	R/W	0	HSP_QMULTIPLY[8:0]	Quantization multiply control is used to compensate for a different weight sum in transposed polyphase or color space matrix mode, remaining bits are fraction (largest number is 511/512). Value range: $0 \leq m < 1.0$. Instead of using values in the range of $m < 0.5$ the quantization shift HSP_QSHIFT should be modified to gain more precision in the truncated result.
15:13		-	Unused	
12:0	R/W	0	HSP_OFFSET_0	Initial start offset for DTO
Offset 0x10 C208			*Initial Zoom delta*	
31:26		-	Unused	
25:0	R/W	0	HSP_DZOOM_0[25:0]	Initial zoom delta for 1 pixel in line (signed, lsb = 2^{-27}) is used for non constant scaling ratios.
Offset 0x10 C20C			*Zoom delta change*	
31:29		-	Unused	
28:0	R/W	0	HSP_DDZOOM[28:0]	Zoom delta change (signed, lsb = 2^{-40}) is used for non-constant scaling ratios.

MEMORY BASED SCALER (MBS) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Color Space Matrix Registers				
Offset 0x10 C220			*Color space matrix coefficients C_{00} - C_{02}*	
31:30		-	Unused	
29:20	R/W	0	CSM_C02[9:0]	Coefficient C02 (signed, LSB = 2^{-9})
19:10	R/W	0	CSM_C01[9:0]	Coefficient C01 (signed, LSB = 2^{-9})
9:0	R/W	0	CSM_C00[9:0]	Coefficient C00 (signed, LSB = 2^{-9})
Note: Signed values are represented as two's complement.				

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MEMORY BASED SCALER (MBS) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 C224			*Color space matrix coefficients C_{10} - C_{12}*	
31:30		-	Unused	
29:20	R/W	0	CSM_C12[9:0]	Coefficient C12 (signed, LSB = 2^{-9})
19:10	R/W	0	CSM_C11[9:0]	Coefficient C11 (signed, LSB = 2^{-9})
9:0	R/W	0	CSM_C10[9:0]	Coefficient C10 (signed, LSB = 2^{-9})
Offset 0x10 C228			*Color space matrix coefficients C_{20} - C_{22}*	
31:30		-	Unused	
29:20	R/W	0	CSM_C22[9:0]	Coefficient C22 (signed, LSB = 2^{-9})
19:10	R/W	0	CSM_C21[9:0]	Coefficient C21 (signed, LSB = 2^{-9})
9:0	R/W	0	CSM_C20[9:0]	Coefficient C20 (signed, LSB = 2^{-9})
Offset 0x10 C22C			*Color space matrix offset coefficients D_0 - D_2*	
31:29		-	Unused	
28	R/W	0	CSM_D2_TWOS	Offset coefficient D_2 type 0 = Unsigned 1 = Signed
27:20	R/W	0	CSM_D2[7:0]	Offset coefficient D_2 (LSB = 2^0)
19		-	Unused	
18	R/W	0	CSM_D1_TWOS	Offset coefficient D_1 type 0 = Unsigned 1 = Signed
17:10	R/W	0	CSM_D1[7:0]	Offset coefficient D_1 (LSB = 2^0)
9		-	Unused	
8	R/W	0	CSM_D0_TWOS	Offset coefficient D_0 type 0 = Unsigned 1 = Signed
7:0	R/W	0	CSM_D0[7:0]	Offset coefficient D_0 (LSB = 2^0)
Offset 0x10 C230			*Color space matrix offset coefficients E_0 - E_2*	
31:30		-	Unused	
29:20	R/W	0	CSM_E2[9:0]	Offset coefficient E2, two's complement (signed, LSB = 2^{-2})
19:10	R/W	0	CSM_E1[9:0]	Offset coefficient E1, two's complement (signed, LSB = 2^{-2})
9:0	R/W	0	CSM_E0[9:0]	Offset coefficient E0, two's complement (signed, LSB = 2^{-2})

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MEMORY BASED SCALER (MBS) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Vertical Video Processing Control Registers				
Offset 0x10 C240			*Initial Zoom*	
31:29	R/W	0	VSP_PHASE_MODE[2:0]	Phase mode 0 = 64 phases 1 = 32 phases 2 = 16 phases 3 = 8 phases 4 = 4 phases 5 = 2 phases 6 = Fixed phase 7 = Linear phase interpolation (valid only for 4 component modes).
28		-	Unused	
27:26	R/W	0	VSP_FIR_COMP[1:0]	Vertical filter components 00 = Two components, 6-tap FIR each* 01 = Two components (alternative tap ratio) 10 = Three components, 4-tap FIR each 11 = Four components, 3-tap FIR each *Filter lengths differ when in de-interlacing mode.
25:20		-	Unused	
19:0	R/W	0	VSP_ZOOM_0[19:0]	Initial zoom for 1st pixel in line (unsigned, LSB = 2^{-16}) 2 0000 (hex) = Downscale 50% 1 0000 (hex) = No scaling = 2^{0} 0 8000 (hex) = Zoom 2 x
Offset 0x10 C244			*Phase Control*	
31		-	Unused	
30:28	R/W	0	VSP_QSHIFT[2:0]	Quantization shift control used to change quantization before being multiplied with VSP_MULTIPLY. 100 (bin) = Divide by 16. 101 (bin) = Divide by 8. 110 (bin) = Divide by 4. 111 (bin) = Divide by 2. 000 (bin) = Multiply by 1. 001 (bin) = Multiply by 2. 010 (bin) = Multiply by 4. 011 (bin) = Multiply by 8.
27:26		-	Unused	
25	R/W	0	VSP_QSIGN	Quantization sign bit
24		-	Unused	
23:21		-	VSP_LDIFF_C[2:0]	Line offset for chroma line count (signed) This setting can be used to manipulate the automatically calculated chroma line count. Usually this setting can be left at zero. (used for 4:2:0 scaling and deinterlacing only)
20:16	R/W	0	VSP_OFFSET_C[12:8]	Initial start offset for chroma DTO (is used for 4:2:0 scaling and de-interlacing only).
15:13		-	Unused	
12:0	R/W	0	VSP_OFFSET_0[12:0]	Initial start offset for DTO
Offset 0x10 C248			*Initial Zoom delta*	
31:26		-	Unused	

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MEMORY BASED SCALER (MBS) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
25:0	R/W	0	VSP_DZOOM_0[25:0]	Initial zoom delta for 1 pixel in line (signed, LSB = 2^{-27}) is used for non-constant scaling ratios
Offset 0x10 C24C			*Zoom delta change*	
31:29		-	Unused	
28:0	R/W	0	VSP_DDZOOM[28:0]	Zoom delta change (signed, LSB = 2^{-40}) is used for non-constant scaling ratios.

MEMORY BASED SCALER (MBS) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Color Keying Control Registers				
Offset 0x10 C280			*Color Key Control*	
31:30	R/W	0	CKEY_K2A	Color key to alpha convert 00 = No alpha manipulation 01 = Fixed alpha at output 10 = Reserved 11 = Color key to alpha convert Alpha value for non-key sample is taken from CKEY_ALPHA register, alpha value for key sample is set to zero.
29:28	R/W	0	CKEY_A2K	Alpha mode to color key convert 00 = No alpha manipulation 01 = Reserved 10 = Reserved 11 = Alpha to color key convert Samples with alpha component below 80 (hex) are replaced with values defined in CKEY_COMP 1-3.
27:26	R/W	0	CKEY_REPLACE	Color keying replace mode 00 = No color component manipulation 01 = Replace keyed color components with black (10, 10, 10.) 10 = Replace keyed color components with gray (80, 80, 80). 11 = Replace keyed color components with last non-key value.
25:24		-	Unused	
23:16	R/W	0	CKEY_MASK1	Color key mask component 1defines bits of color component that are compared against color key value setting to key sample.
15:8	R/W	0	CKEY_MASK2	Color key mask component 2 defines bits of color component that are compared against color key value setting to key sample.
7:0	R/W	0	CKEY_MASK3	Color key mask component 3 defines bits of color component that are compared against color key value setting to key sample.
Offset 0x10 C284			*Color Key Components*	
31:24	R/W	0	CKEY_ALPHA	Alpha value defines the alpha value to be used for keyed samples.
23:16	R/W	0	CKEY_COMP1	Color key component 1 defines value of color key for component 1 (red or Y).
15:8	R/W	0	CKEY_COMP2	Color key component 2 defines value of color key for component 2 (green or U).
7:0	R/W	0	CKEY_COMP3	Color key component 3 defines value of color key for component 3 (blue or V).

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MEMORY BASED SCALER (MBS) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Video Output Format Control Registers				
Offset 0x10 C300			*Video Output Format*	
31:30	R/W	0	PSU_BAMODE	Base address mode 00 = Single set (e.g, progressive video source) base 1-3 according to number of planes (plane 1-3) 01 = Alternate sets each line (e.g. anti-flicker mode) base 1-3, first line out, etc. (plane 1-3) base 4-6, second line out, etc. (plane 1-3) 1x = Reserved
29:14		-	Unused	
13	R/W	0	PSU_ENDIAN	Output format Endianness 0 = Same as system Endianness 1 = Opposite of system Endianness
12		-	Unused	
11:10	R/W	0	PSU_DITHER	Output format dither mode 00 = No dithering 01 = Error dispersion (never reset pattern). 10 = Error dispersion (reset pattern at startup). 11 = Error dispersion (reset pattern every field.)
9:8	R/W	0	PSU_ALPHA	Output format alpha mode 00 = No alpha (alpha byte is not written to memory). 01 = Alpha byte written (see Color Keying Control). 10 = Reserved 11 = Reserved
7:0	R/W	0	PSU_OPFMT	Output formats 00 (hex) = YUV 4:2:0, semi-planar 03 (hex) = YUV 4:2:0, planar 08 (hex) = YUV 4:2:2, semi-planar 0B (hex) = YUV 4:2:2, planar 0F (hex) = RGB or YUV 4:4:4, planar A9 (hex) = Compressed 4/4/4 + (4-bit alpha) AA (hex) = Compressed 4/5/3 + (4-bit alpha) AD (hex) = Compressed 5/6/5 A0 (hex) = Packed YUY2 4:2:2 A1 (hex) = Packed UYVY 4:2:2 E2 (hex) = YUV or RGB 4:4:4 + (8-bit alpha) E3 (hex) = VYU 4:4:4 + (8-bit alpha)
Offset 0x10 C304			*Target Window Size*	
31:27		-	Unused	
26:16	R/W	0	PSU_LSIZE	Line size is used for horizontal cropping after scaling: 0 = Cropping disabled. 1 = One pixel
15:11		-	Unused	
10:0	R/W	0	PSU_LCOUNT	Line count is used for vertical cropping after scaling: 0 = Cropping disabled. 1 = One line

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MEMORY BASED SCALER (MBS) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Video Output Address Generation Control Registers				
Offset 0x10 C340			*Target Base Address #1*	
31:26		-	Unused	
25:3	R/W	0	PSU_BASE1	Base address DMA #1, used depending on PSU_BAMODE setting.
2:0	R/W	0	PSU_OFFSET1	Base address byte offset DMA #1 bits define pixel offset within multi pixel 64-bit words (e.g., a 16-bit pixel can be placed on any 16-bit boundary).
Offset 0x10 C344			*Target Line Pitch #1*	
31:15		-	Unused	
14:3	R/W	0	PSU_PITCH1	Line pitch DMA #1, signed value (two's complement) is used for all packed formats and for plane 1.
2:0		-	Unused	
Offset 0x10 C348			*Target Base Address #2*	
31:26		-	Unused	
25:3	R/W	0	PSU_BASE2	Base address DMA #2, used depending on PSU_BAMODE setting.
2:0	R/W	0	PSU_OFFSET2	Base address byte offset DMA #2 bits define pixel offset within multi pixel 64-bit words (e.g., a 16-bit pixel can be placed on any 16-bit boundary).
Offset 0x10 C34C			*Target Line Pitch #2*	
31:15		-	Unused	
14:3	R/W	0	PSU_PITCH2	Line pitch DMA #2, signed value (two's complement) is used for planes 2 and 3.
2:0		-	Unused	
Offset 0x10 C350			*Target Base Address #3*	
31:26		-	Unused	
25:3	R/W	0	PSU_BASE3	Base address DMA #3, used depending on PSU_BAMODE setting.
2:0	R/W	0	PSU_OFFSET3	Base address byte offset DMA #3 bits define pixel offset within multi pixel 64-bit words (e.g., a 16-bit pixel can be placed on any 16-bit boundary).
Offset 0x10 C354			*Target Base Address #4*	
31:26		-	Unused	
25:3	R/W	0	PSU_BASE4	Base address DMA #4, used depending on PSU_BAMODE setting.
2:0		-	Unused	
Offset 0x10 C358			*Target Base Address #5*	
31:26		-	Unused	
25:3	R/W	0	PSU_BASE5	Base address DMA #5, used depending on PSU_BAMODE setting.
2:0		-	Unused	
Offset 0x10 C35C			*Target Base Address #6*	

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MEMORY BASED SCALER (MBS) REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
31:26		-	Unused	
25:3	R/W	0	PSU_BASE6	Base address DMA #6, used depending on PSU_BAMODE setting.
2:0		-	Unused	

MEMORY BASED SCALER (MBS) REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Miscellaneous Registers				
Offset 0x10 C400—C7FC Color Look-Up Table				
31:24	W	NI	LUT_ALPHA[x]	Alpha
23:16	W	NI	LUT_RED[X][7:0]	Red or Y
15:8	W	NI	LUT_GREEN[X][7:0]	Green or U
7:0	W	NI	LUT_BLUE[X][7:0]	Blue or V
Offset 0x10 C800—C9FC Coefficient Table #1 Taps 0-5 (Horizontal) (64 entries x 64 bits)				
63:62		-	Unused	
61:52	W	NI	TAP_5[X][9:0]	Inverted coefficient tap #5, two's complement
51:42	W	NI	TAP_4[X][9:0]	Inverted coefficient tap #4, two's complement
41:32	W	NI	TAP_3[X][9:0]	Inverted coefficient tap #3, two's complement
31:30		-	Unused	
29:20	W	NI	TAP_2[X][9:0]	Inverted coefficient tap #2, two's complement
19:10	W	NI	TAP_1[X][9:0]	Inverted coefficient tap #1, two's complement
9:0	W	NI	TAP_0[X][9:0]	Inverted coefficient tap #0, two's complement
Offset 0x10 CA00—CBFC Coefficient Table #2 Taps 0-5 (Vertical - Luma) (64 entries x 64 bits)				
63:62		-	Unused	
61:52	W	NI	TAP_5[X][9:0]	Inverted coefficient tap #5, two's complement
51:42	W	NI	TAP_4[X][9:0]	Inverted coefficient tap #4, two's complement
41:32	W	NI	TAP_3[X][9:0]	Inverted coefficient tap #3, two's complement
31:30		-	Unused	
29:20	W	NI	TAP_2[X][9:0]	Inverted coefficient tap #2, two's complement
19:10	W	NI	TAP_1[X][9:0]	Inverted coefficient tap #1, two's complement
9:0	W	NI	TAP_0[X][9:0]	Inverted coefficient tap #0, two's complement
Offset 0x10 CC00—CDFC Coefficient Table #3 Taps 0-5 (Vertical - Chroma) (64 entries x 64 bits)				
63:62		-	Unused	
61:52	W	NI	TAP_5[X][9:0]	Inverted coefficient tap #5, two's complement
51:42	W	NI	TAP_4[X][9:0]	Inverted coefficient tap #4, two's complement
41:32	W	NI	TAP_3[X][9:0]	Inverted coefficient tap #3, two's complement
31:30		-	Unused	

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MEMORY BASED SCALER (MBS) REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
29:20	W	NI	TAP_2[X][9:0]	Inverted coefficient tap #2, two's complement
19:10	W	NI	TAP_1[X][9:0]	Inverted coefficient tap #1, two's complement
9:0	W	NI	TAP_0[X][9:0]	Inverted coefficient tap #0, two's complement

MEMORY BASED SCALER (MBS) REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Interrupt and Status Control Registers				
Offset 0x10 CFE0			*Interrupt Status*	
31:30	R	0	STAT_PSU[1:0]	Status of pixel store unit (test signal)
29:27		-	Unused	
26:16	R	0	STAT_PSU_LINE	Status of pixel store unit, line currently written
15:14	R	0	STAT_VSP[1:0]	Status of vertical scale pipe (test signal)
13:12	R	0	STAT_DFF[1:0]	Status of decimation FIR filter (test signal)
11:10	R	0	STAT_HSP[1:0]	Status of vertical scale pipe (test signal)
9:8	R	0	STAT_IFF[1:0]	Status of interpolation FIR filter (test signal)
7:6	R	0	STAT_PFU[1:0]	Status of pixel fetch unit (test signal)
5	R	0	STAT_TASK_ERROR	Processing error
4	R	0	STAT_TASK_END	Current task processing done
3	R	0	STAT_TASK_OVERFLOW	Task FIFO overflow
2	R	0	STAT_TASK_IDLE	Task finished and task FIFO is empty.
1	R	0	STAT_TASK_EMPTY	Task FIFO runs empty.
0	R	0	STAT_TASK_DONE	Current task finished and all writes are complete.
Offset 0x10 CFE4			*Interrupt Enable*	
31:6		-	Unused	
5	R	0	IEN_TASK_ERROR	Processing error
4	R	0	IEN_TASK_END	Current task processing done
3	R/W	0	IEN_TASK_OVERFLOW	Task FIFO overflow
2	R/W	0	IEN_TASK_IDLE	Task finished and task FIFO is empty.
1	R/W	0	IEN_TASK_EMPTY	Task FIFO runs empty.
0	R/W	0	IEN_TASK_DONE	Current task finished and all writes are complete.
Offset 0x10 CFE8			*Interrupt Clear*	
31:6		-	Unused	
5	R	0	CLR_TASK_ERROR	Processing error
4	R	0	CLR_TASK_END	Current task processing done
3	W	0	CLR_TASK_OVERFLOW	Task FIFO overflow
2	W	0	CLR_TASK_IDLE	Task finished and task FIFO is empty.

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MEMORY BASED SCALER (MBS) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
1	W	0	CLR_TASK_EMPTY	Task FIFO runs empty.
0	W	0	CLR_TASK_DONE	Current task finished and all writes are complete.
Offset 0x10 CFEC			*Interrupt Set*	
31:6		-	Unused	
5	R	0	SET_TASK_ERROR	Processing error
4	R	0	SET_TASK_END	Current task processing done
3	W	0	SET_TASK_OVERFLOW	Task FIFO overflow
2	W	0	SET_TASK_IDLE	Task finished and task FIFO is empty.
1	W	0	SET_TASK_EMPTY	Task FIFO runs empty.
0	W	0	SET_TASK_DONE	Current task finished and all writes are complete.
Offset 0x10 CFF4			*POWERDOWN*	
31	R/W	0	POWER_DOWN	Powerdown register for the module 0 = Normal operation of the peripheral. This is the reset value. 1 = Module is powered down and module clock can be removed. At powerdown, module responds to all reads with DEADABBA (except for reads of powerdown bit) and all writes with ERR ACK (except for writes to powerdown bit).
30:0		-	Unused	Ignore during writes and read as zeroes.
Offset 0x10 CFFC			*Module ID*	
31:16	R	0x0119	MOD_ID	Module ID
15:12	R	0	REV_MAJOR	Major revision counter
11:8	R	1	REV_MINOR	Minor revision counter
7:0	R	0	APP_SIZE	Aperture Size 0 = 4kB

TPI Null 1 Module Registers

TPI NULL 1 MODULE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 DFFC			*Module ID Register*	
31:16	R	0x0124	MOD_ID	Module ID Number
15:12	R	0	REV_MAJOR	Major revision
11:8	R	0	REV_MINOR	Minor revision
7:0	R	0	APP_SIZE	Aperture size is 0 = 4 kB.

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AICP 1 Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.28)

ADVANCED IMAGE COMPOSITION PROCESSOR 1 (AICP) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Screen Timing Generator Registers				
Offset 0x10 E000			*TOTAL*	
31:28		-	Unused	
27:16	R/W	0	HTOTAL	Horizontal Total sets the number of horizontal pixels for the display. Total # of pixels per line = HTOTAL+1.
15:12		-	Unused	
11:0	R/W	0	VTOTAL	Vertical Total sets the number of vertical pixels for the display. Total # of lines per field = VTOTAL +1.
Offset 0x10 E004			*HBLANK*	
31:28		-	Unused	
27:16	R/W	0	HBLANKS	Horizontal Blank Start sets the pixel location where horizontal blanking starts.
15:12		-	Unused	
11:0	R/W	0	HBLNKE	Horizontal Blank End sets the pixel location where horizontal blanking ends.
Offset 0x10 E008			*VBLANK*	
31:28		-	Unused	
27:16	R/W	0	VBLANKS	Vertical Blank Start sets the pixel location where vertical blanking starts.
15:12		-	Unused	
11:0	R/W	0	VBLANKE	Vertical Blank End sets the pixel location where vertical blanking ends.
Offset 0x10 E00C			*HSYNC*	
31:28		-	Unused	
27:16	R/W	0	HSYNCS	Horizontal Sync Start sets the pixel location where horizontal sync starts.
15:12		-	Unused	
11:0	R/W	0	HSYNCE	Horizontal Sync End sets the pixel location where horizontal sync ends.
Offset 0x10 E010			*VSYNC*	
31:28		-	Unused	
27:16	R/W	0	VSYNCS	Vertical Sync Start sets pixel location where Vertical sync starts.
15:12		-	Unused	
11:0	R/W	0	VSYNCE	Vertical Sync End sets pixel location where Vertical sync ends.

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ADVANCED IMAGE COMPOSITION PROCESSOR 1 (AICP) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Control and Interrupt Registers				
Offset 0x10 E014			*VINTERRUPT*	
31:28		-	Unused	
27:16	R/W	0	VLINTA	Vertical Line Interrupt A sets a vertical line number where an interrupt will be generated when the scanline matches this value. The interrupt is monitored by the Event Monitor (EVM).
15:12		-	Unused	
11:0	R/W	0	VLINTB	Vertical Line Interrupt B sets a vertical line number where an interrupt will be generated when the scanline matches this value. The interrupt is monitored by the Event Monitor (EVM).
Offset 0x10 E018			*FEATURES*	
31:5		-	Unused	
4:3	R	0x1	NOGAMMALUTS	Number of gamma LUTS binary coded for the output channels (The first slice of the AICP out goes through the gamma LUT.): Value for AICP1 is 0x1.
2:0	R	0x4	NOLAYERS	Number of layers in this AICP: Value for AICP1 is 0x4.
Note: For the interrupt to occur, it must be enabled in the STG control register.				
Offset 0x10 E01C			*STATUS*	
31		-	Unused	
30	R	0	O_E_STAT	Odd/Even flag status (interlaced mode) 0 = First field (odd) 1 = Second field (even)
29	R	0	VSYNCSTAT	Read back current status of VSYNC 0 = Not in Vertical Sync area 1 = Sweep is in Vertical Sync.
28	R	0	VBLNKSTAT	Read back current status of VBLANK 0 = Not in Vertical Blanking area 1 = Sweep is in Vertical Blanking.
27:16	R	0	YCNT	Read back line current count
15:12		-	Unused	
11:0	R	0	XCNT	Read back position in current line
Offset 0x10 E020			*CONTROL*	
31:30		-	Unused	
29	R/W	0	Interlaced	Interlaced mode bit 0 = Non-interlaced mode; VTotal=frame height. 1 = Interlaced mode Field height = VTotal+1 for odd fields. Field height = VTotal for even fields.
28	R/W	0	BlankPol	BLANK Polarity 0 = Positive blank 1 = Negative blank
27		-	Unused	

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ADVANCED IMAGE COMPOSITION PROCESSOR 1 (AICP) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
26	R/W	0	HSYNCPol	HSYNC Polarity 0 = Positive going 1 = Negative going
25		-	Unused	
24	R/W	0	VSYNCPol	VSYNC Polarity 0 = Positive going 1 = Negative going
23:21		-	Unused	
20	R/W	0	BlankCtl	Blank Control allows either normal blanking or forces blanking to occur immediately. 0 = Force Blank 1 = Normal Blank
19		-	Unused	
18	R/W	0	HSYNCCtl	HSYNC Control enables or disables the horizontal sync output of the chip. 0 = Disable 1 = Enable
17		-	Unused	
16	NI	0	VSYNCCtl	VSYNC Control enables or disables vertical sync output of the chip. 0 = Disable 1 = Enable
15:3		-	Unused	
2	R/W	0x1	TRIGGER_POL	External trigger polarity 1 = Positive edge (default) 0 = Negative edge
1	R/W	0	MASTER	STG master/slave/operation 0 = Master mode 1 = Slave mode
0	R/W	0	TGRST	Timing generator reset 0 = Disable 1 = Enable Disable will reset all layer_enable bits (global AICP reset).
Offset 0x10 E028			*INTLCTRL1*	
31:28		-	Unused	
27:16	R/W	0	INT_START_E	Horizontal offset for VSYNC start even field (interlaced mode only) Vsync appears at INT_START_E + 1.
15:12		-	Unused	
11:0	R/W	0	INT_START_O	Horizontal offset for VSYNC start odd field (interlaced mode only) Vsync appears at INT_START_O + 1.
Offset 0x10 E02C			*INTLCTRL2*	
31:28		-	Unused	
27:16	R/W		INT_END_E	Horizontal offset for VSYNC end even field (interlaced mode only)
15:12		-	Unused	
11:0	R/W	0	INT_END_O	Horizontal offset for VSYNC end odd field (interlaced mode only)
Offset 0x10 E030			*VBI SRC Address*	
31:26		-	Unused	

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ADVANCED IMAGE COMPOSITION PROCESSOR 1 (AICP) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
25:0	R/W	0	VBI_SRC_ADDR	VBI data source address
Offset 0x10 E034			*VBI_CTRL*	
31:1		-	Unused	
0	R/W	0	VBI_EN	Enable VBI data fetch engine.
Offset 0x10 E038			*VBI_SENT_OFFSET*	
31:12		-	Unused	
11:0	R/W	0	VBI_SENT_OFFSET	This programming value specifies the number of lines to add to the linecnt value in the packet identifier.
Offset 0x10 E03C			*OUT_CTRL*	
31:20			Unused	
19	R/W	1	10Bit	1 = output formatter works in 10 bit per color component mode 0 = output formatter works in 8 bit per color component mode
18	R/W	0	qualifier	1 = slice qualifier is put out 0 = hsync is put out
17:16	R/W	0	outmode	00 = output interface runs is two-d1 mode 01 = output interface runs in double-d1 mode 10 = output interface operates in 24bit parallel mode 11 = unused
15	R/W	0	parallel_mode	This bit controls the sync delay compensation. 1 = syncs are delayed (needed for 24bit parallel output mode) 0 = no additional sync delay
14	R/W	1	TC_outS2	1 = invert the MSB of the second D1 slice 0 = leave second D1 slice untouched
13	R/W	1	TC_outS1	1 = invert the MSB of the first D1 slice 0 = leave first D1 slice untouched
12	R/W	0	oversample	This bit enables the output state machine for oversampling. This bit should be 0 for interleaved output modes. If one (only supported for a single d1 stream, either 444 or 422 or 444x) the output clock should be 2x the streaming clock i.e. 422 SD mode: streaming clock 27Mhz, output clock 54Mhz results in a 2x oversampling of the data stream. 1 = oversampling enabled 0 = no oversampling
11	R/W	0	RGBX	1 = RGBX/YUVX mode 0 = RGB/YUV mode
10	R/W	1	D1_MODE	1 = 4:2:2 D1 mode 0 = 4:4:4 D1 mode
9	R/W	0	INTERLEAVE	1 = Interleaved mode (2 D1 streams are interleaved clk_icp_interl must be set to 2x clk_icp_mux) 0 = non interleaved mode
8	R/W	0	SLICE_SEL	Interleaved mode: determines the position of the two slices in the stream. Non-interleaved mode: determines which of the selected slices goes in the stream. 0 = Mux_sel_1 1 = Mux_sel_2
7:6			Unused	

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ADVANCED IMAGE COMPOSITION PROCESSOR 1 (AICP) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
5:4	R/W	0	MUX_SEL_2	Tap off selection for second slice 0 = tap off after first mixing stage 1 = tap off after second mixing stage 2 = tap off after third mixing stage(AICP1 ONLY) 3 = tap off after fourth mixing stage (AICP1 ONLY)
3:2			Unused	
1:0	R/W	0	MUX_SEL_1	Tap off selection for first slice 0 = tap off after first mixing stage 1 = tap off after second mixing stage 2 = tap off after third mixing stage(AICP1 ONLY) 3 = tap off after fourth mixing stage (AICP1 ONLY)
Offset 0x10 E040			*OUTPUT GAMMA LUT CTRL (AICP1 ONLY)*	
31:30			Unused	
29:20	R/W	0	LUT_RED	Gamma LUT data port red This register reads always 0 if the “Host_Enable” bit is 0
19:10	R/W	0	LUT_GREEN	Gamma LUT data port green This register reads always 0 if the “Host_Enable” bit is 0
9:0	R/W	0	LUT_BLUE	Gamma LUT data port blue This register reads always 0 if the “Host_Enable” bit is 0
Offset 0x10 E044			*GAMMA LUT CTRL (AICP1 ONLY)*	
31	R/W	0	LUT_ENABLE	Gamma LUT enable bit 1 = Active 0 = Bypass
30	R/W	0	HOST_ENABLE	This bit enables Host read/write access to the LUT: 1 = Host access enabled. 0 = Host access disabled, no access possible.
29:25		-	Unused	
24:16	R/W	0	LUT_ADDR	Gamma LUT address, no auto increment supported.
15:1		-	Unused	
0	R/W	0	LUT_RW	Gamma LUT read/write 1 = Write access to gamma LUT 0 = Read access to gamma LUT
Offset 0x10 E050			*Signature1*	
31:16	R	0	middle signature	Middle path signature
15:0	R	0	lower signature	Lower path signature
Offset 0x10 E054			*Signature2*	
31:16	R	0	alpha signature	Alpha path signature
15:0	R	0	upper signature	Upper path signature
Offset 0x10 E058			*Signature3*	
31:16	R	0	misc signature	Other signature
15:9		-	Unused	
8	R	0	sig_done	Signature done
7:6		-	Unused	

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ADVANCED IMAGE COMPOSITION PROCESSOR 1 (AICP) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
5:4	R/W	0	sig_select	Signature select
3:1		-	Unused	
0	R/W	0	sig_enable	Signature enable

ADVANCED IMAGE COMPOSITION PROCESSOR 1 (AICP) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Layer & Mixer Registers				
The structure of each layer function block is identical. The register for a function such as Source Address in Layer 1, has the same structure as the corresponding register in Layer 2 to Layer 4. Layer one starts at offset 0x100 from the AICP base address Layer two starts at offset 0x200 from the AICP base address Layer three (AICP1 only) starts at offset 0x300 from the AICP base address Layer four (AICP1 only) starts at offset 0x400 from the AICP base address				
Offset 0x10 E100			*Layer Source Address A*	
31:26		-	Unused	
25:0	R/W	0	Layer N Source Address A	Layer N Source Data Start Address A in bytes. This sets starting address A for data transfers from the linear Frame Buffer memory to Layer N. **Note:** It should be aligned on a 128-byte boundary for memory performance reasons. It has to be 8-byte aligned.
Offset 0x10 E104			*Layer Pitch A*	
31:23		-	Unused	
22:0	R/W	0	Layer N Pitch A	Layer N Source Data Pitch B in bytes. This sets pitch A for data transfers from the linear Frame Buffer memory to Layer N. The value has to be rounded up to the next 64-bit word.
Offset 0x10 E108			*Layer Source Width A*	
31:23		-	Unused	
22:0	R/W	0	Layer N Source Width A	Layer N source width in bytes A. The value has to be rounded up to the next 64-bit word.
Offset 0x10 E10C			*Layer Source Address B*	
31	W	0	Source address upload	Writing a 1 to this bit will initiate an address upload of layer source address a and b into the register shadow area.
30:26		-	Unused	
25:0	R/W	0	Layer N Source Address B	Layer N Source Data Start Address B in bytes. This sets starting address B for data transfers from the linear Frame Buffer memory to Layer N. **Note:** It should be aligned on a 128-byte boundary. It has to be 8-byte aligned.
Offset 0x10 E110			*Layer Pitch B*	
31:23		-	Unused	
22:0	R/W	0	Layer N Pitch B	Layer N Source Data Pitch B in bytes sets pitch B for data transfers from the linear Frame Buffer memory to Layer N. The value has to be rounded up to the next 64-bit word.

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ADVANCED IMAGE COMPOSITION PROCESSOR 1 (AICP) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 E114			*Layer Source Width B*	
31:23		-	Unused	
22:0	R/W	0	Layer Source Width B	Layer N source width in bytes B. The value has to be rounded up to the next 64-bit word.
Offset 0x10 E130			*Layer Start*	
31	R/W	0	Fine	Fine positioning enable for interlaced modes (layer size needs to be set to odd + even number of lines). This feature should only be used for graphic contents as it is changing the temporal relationship between subsequent fields. If fine positioning is enabled, the entire layer must be completely positioned within the visible screen area. Cropping has to be performed by setting the layer dimensions and position to the appropriate values.
30:29		-	Unused	
28:16	R/W	0	LayerNStartX	Layer N Start x position (from zero at left edge) in pixels.
15:13		-	Unused	
12:0	R/W	0	LayerNStartY	Layer N Start y position (from zero at top) in lines.
Offset 0x10 E134			*Layer Size*	
31:28		-	Unused	
27:16	R/W	0	LayerNHeight	Layer N height in lines.
15:12		-	Unused	
11:0	R/W	0	LayerNWidth	Layer N width, in pixels.
Offset 0x10 E138			*Layer Pixel Format*	
31	R/W	0x1	LayerExpansionParameter	Controls how data that is not 24-bit data is converted to 24-bit data when necessary. 0 =Use source data left-aligned into msbits and fill lsbits with 0s. 1 = Use source data left-aligned into msbits and replicate highest msb data into remaining lower order bits.
30	R/W	0	Indexed	0 = No indexed colors, CLUT is shut off. 1 = Indexed colors
29:24	R/W	0	Offset	6-bit offset value specifies how many bits to offset in the first-fetched Long Word at the beginning of a line.
23:16	R/W	0	LayerNFixedAlphaValue	Alpha blend value to be applied in Mixer. This 8-bit field provides 256 levels of fixed alpha-blending. The AlphaSelect ROP must be set appropriately to use this feature.
15:14	R/W	0	Alpha	00 = No Alpha information in pixel data 01 = 4-bit Alpha information in pixel data 10 = 8-bit Alpha information in pixel data 11 = Reserved
13:8	R/W	0	Bits Per Pixel	The total number of bits per pixel needs to be specified here. This number has to include potential alpha bits or unused bits for unpacked formats.
7	R/W	0	Premult	If this bit is set, the incoming pixels are premultiplied with alpha. That disables the new x alpha multiplication in the mixer stage if alpha-blending is enabled.

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ADVANCED IMAGE COMPOSITION PROCESSOR 1 (AICP) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
6:4	R/W	0	Channel Swap/UV_Swap	Ext/Int channel relationship (assignment of A/Y/U/V or A/R/G/B to alpha/upper/middle/lower AICP layer processing channel). 000 = (A)UML - yvyu/vyuy 001 = (A)ULM - yuyv/uyvy 010 = (A)MUL 011 = (A)MLU 100 = (A)LUM 101 = (A)LMU 110 = M(A)UL 111 = L(A)UM Swaps the UV pixel information in the pixel formatter for 4:2:2 formats to provide YVYU and YUYV formats.
3:0	R/W	0	Mux Order	Non-Indexed Mode determines how the bits within a pixel are assigned to the rgb/yuv channels. 0000 = mode_332 0001 = mode_444 0010 = mode_534 0011 = mode_555 0100 = mode_565 0101 = mode_633 0110 = mode_888 0111 = mode_vyuy 1110 = mode_yvyu Indexed Mode specifies the actual index size without alpha i.e., 2bpp indexed = 4'b0010 Note: In indexed mode the following formula should be satisfied: BPP >= Mux_Order + Alpha x 4.
Offset 0x10 E13C			*Layer Pixel Processing*	
31	R/W	0	pu2c	Controls the upper previous channel format input to the mixer. 0 = Data left untouched. 1 = Data conversion two's complement <-> binary offset
30	R/W	0	pm2c	Controls the middle previous channel format input to the mixer. 0 = Data left untouched. 1 = Data conversion two's complement <-> binary offset
29	R/W	0	pl2c	Controls the lower previous channel format input to the mixer. 0 = Data left untouched. 1 = Data conversion two's complement <-> binary offset
28	R/W	0	cu2c	Controls the upper current channel format input to the mixer. 0 = Data left untouched. 1 = Data conversion two's complement <-> binary offset
27	R/W	0	cm2c	Controls the middle current channel format input to the mixer. 0 = Data left untouched. 1 = Data conversion two's complement <-> binary offset
26	R/W	0	cl2c	Controls the lower current channel format input to the mixer. 0 = Data left untouched. 1 = Data conversion two's complement <-> binary offset
25	R/W	0	ou2c	Controls the upper channel format output of the mixer. 0 = Data left untouched. 1 = Data conversion two's complement <-> binary offset
24	R/W	0	om2c	Controls the middle channel format output of the mixer. 0 = Data left untouched. 1 = Data conversion two's complement <-> binary offset

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ADVANCED IMAGE COMPOSITION PROCESSOR 1 (AICP) REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
23	R/W	0	ol2c	Controls the lower channel format output of the mixer. 0 = Data left untouched. 1 = Data conversion two's complement <-> binary offset
22:20	R/W	0	endianness swap	This specifies the used endianness swapping: 000 = swapping is controlled by bits per pixel and global endianness signal. The incoming 32 bits are interpreted as byte order "4321". Swapping will look like: 100 = No swapping 101 = 3412 110 = 2143 111 = 1234
19	R/W	0	Alpha_index	1 = Take incoming pixel value and put it into the alpha channel. 0 = No alpha indexing, take a separate value according to pixel format specification.
18	R/W	0	Alpha_mix	Enables alpha scaling. 0 = Switched off 1 = Per pixel alpha is multiplied with (fixed_alpha)/256.
17		-	Unused	
16	R/W	0	Alpha_use	Controls which alpha value is used for blending in the layer mixer stage 1 = Use previous alpha 0 = Use alpha of current layer
15:13		-	Unused	
12	R/W	0	A2C	Controls the alpha channel format within a layer. 0 = Data left untouched. 1 = Data conversion two's complement <-> binary offset
11	R/W	0	U2C	Controls the upper data channel format within a layer. 0 = Data left untouched. 1 = Data conversion two's complement <-> binary offset
10	R/W	0	M2C	Controls the middle data channel format within a layer. 0 = Data left untouched. 1 = Data conversion two's complement <-> binary offset
9	R/W	0	L2C	Controls the lower data channel format within a layer. 0 = Data left untouched. 1 = Data conversion two's complement <-> binary offset
8	R/W	0	LUT_Enable	This bit enables the LUT. 0 = LUT is bypassing pixel. 1 = Use output of the LUT.
7:6		-	Unused	
5	R/W	0	Upsample	Up-sample filter enable 0 = Bypass 1 = Up-sample filter is enabled. Works on two's complement 422 co-sited data.
4	R/W	0	422_444_en	This bit works in conjunction with the shift_en bit. If it is enabled, it converts 422 interspersed data into 444 data. Shift_en has to be switched on. 0 = Bypass 1 = Enable
3	R/W	0	Shift_en	This bit enables a filter to convert 422 interspersed data into 422 co-sited data. 0 = Bypass 1 = Enable

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ADVANCED IMAGE COMPOSITION PROCESSOR 1 (AICP) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
2:1		-	Unused	
0	R/W	0	Bandlimit	This bit specifies if the band limiting filter and subsampler for 444 to 422 conversion is switched on. 0 = No band limiting/subsampling applied in the data path. 1 = Apply band limiting/subsampling.
Offset 0x10 E140			*Layer Status/Control*	
31:27		-	Unused	
26	R	0	Layer_FUSF_Status	Layer FIFO Underflow Status. Read 0 = No Underflow Read 1 = Underflow took place Write 1 to clear Underflow Status.
25:12		-	Unused	
11	R	NI	Address upload	This bit indicates if a fetch start address upload is currently in progress: 1 = Upload is in progress, do not reprogram source addr a or b. 0 = Upload is done, reprogramming is safe.
10	R/W	0	Buffer toggle	This bit controls the dma buffer mode: 1 = Always toggle between buffer A and B (A=odd field, B=even field). 0 = No buffer toggle, always fetch from buffer spec A.
9	R	NI	Layer upload	This bit indicates if the register upload into the shadow area is still in progress. 1 = Upload is in progress. 0 = Upload done.
8	R	0	Layer_recover	0 = Layer doesn't recover after detecting a FIFO underflow. 1 = Layer recovers after FIFO underflow.
7:6		-	Unused	
5	R	1	DownFilter	0 = Layer does not contain an 4:4:4 to 4:2:2 down filte.r 1 = Layer contains an 4:4:4 to 4:2:2 down filter.
4	R	1	UpsampleFilter	0 = Layer does not contain an 4:2:2 to 4:4:4 up-sampling filter. 1 = Layer contains an 4:2:2 to 4:4:4 up-sampling filter.
3	R	1	CSC	0 = Layer does not contain a color space matrix. 1 = Layer contains a color space matrix.
2	R	1	AlphaLUT	0 = Layer does not contain the Alpha LUT. 1 = Layer contains the Alpha LUT.
1	R	1	ComponentLUT	0 = Layer does not contain the RGB/YUV component LUTs. 1 = Layer contains the RGB/YUV component LUTs.
0	R/W	0	LayerN_Enable	0 = Disable layer N 1 = Enable layer N This register reads always 0 if the screen timing generator is not enabled
Offset 0x10 E144			*LUT Programming*	
31:24	R/W	0	Alpha	Alpha value for LUT programming This register reads always 0 if the "Host_Enable" bit is 0
23:16	R/W	0	Red	Red value for LUT programming This register reads always 0 if the "Host_Enable" bit is 0
15:8	R/W	0	Green	Green value for LUT programming This register reads always 0 if the "Host_Enable" bit is 0

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ADVANCED IMAGE COMPOSITION PROCESSOR 1 (AICP) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
7:0	R/W	0	Blue	Blue value for LUT programming This register reads always 0 if the “Host_Enable” bit is 0
Offset 0x10 E148			*LUT Addressing*	
31:24	R/W	0	LUTAddress	Address register for LUT programming, no auto-increment is supported.
23:9		-	Unused	
8	R/W	0	Host_Enable	This enables read/write access by the host: 1 = Host access enabled. 0 = Host access disabled.
7:1		-	Unused	
0	R/W	0	Read/Write	0 = Read 1 = Write
Offset 0x10 E14C			*Mixer Pixel Key AND Register*	
31:24	R/W	0xFF	PixelKeyAND	The bits 31:24 in 32 bpp mode are ANDed with this mask (input for KEY2).
23:0		-	Unused	
Offset 0x10 E150			*Color Key1 AND Mask*	
31:24		-	Unused	
23:0	R/W	0xFFFFFF	ColorKeyAND1	Defines a 24-bit Mask where the pixel is ANDed before it’s keyed with the ColorKeyAND value.
Offset 0x10 E154			*Color Key Up1*	
31:24		-	Unused	
23:0	R/W	0	ColorKeyup1	Defines a 24-bit color key used for color keying inside the layer.
Offset 0x10 E158			*Color Key Low1*	
31:24		-	Unused	
23:0	R/W	0	ColorKeylow1	Defines a 24-bit color key used for color keying inside the layer.
Offset 0x10 E15C			*Color Key Replace1*	
31	R/W	0	Colorkeyreplaceen	Enables color replacement.
30:24		-	Unused	
23:0	R/W	0	ColorKeyreplace1	Defines a 24-bit color to be put into the data path if the color key matches.
Offset 0x10 E160			*Color Key2 AND Mask*	
31:24		-	Unused	
23:0	R/W	0xFFFFFF	ColorKeyAND2	Defines a 24-bit Mask where the pixel is ANDed before it’s keyed with the COLORKEY value.
Offset 0x10 E164			*Color Key Up2*	
31:24		-	Unused	
23:0	R/W	0	ColorKeyup2	Defines a 24-bit color key used for color keying inside the layer.
Offset 0x10 E168			*Color Key Low2*	
31:24		-	Unused	
23:0	R/W	0	ColorKeylow2	Defines a 24-bit color key used for color keying inside the layer.

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ADVANCED IMAGE COMPOSITION PROCESSOR 1 (AICP) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 E16C			*Color Key Replace2*	
31	R/W	0	Colorkeyreplaceen	Enables color replacement.
30:24		-	Unused	
23:0	R/W	0	ColorKeyreplace2	Defines a 24-bit color to be put into the data path if the color key matches.
Offset 0x10 E170			*Color Key3 AND Mask*	
31:24		-	Unused	
23:0	R/W	0xFFFFFF	ColorKeyAND3	Defines a 24-bit Mask where the pixel is ANDed before it's keyed with the COLORKEY value.
Offset 0x10 E174			*Color Key Up3*	
31:24		-	Unused	
23:0	R/W	0	ColorKeyup3	Defines a 24-bit color key used for color keying inside the layer.
Offset 0x10 E178			*Color Key Low3*	
31:24		-	Unused	
23:0	R/W	0	ColorKeylow3	Defines a 24-bit color key used for color keying inside the layer.
Offset 0x10 E17C			*Color Key Replace3*	
31	R/W	0	Colorkeyreplaceen	Enables color replacement.
30:24		-	Unused	
23:0	R/W	0	ColorKeyreplace3	Defines a 24-bit color to be put into the data path if the color key matches.
Offset 0x10 E180			*Color Key4 AND Mask*	
31:24		-	Unused	
23:0	R/W	0xFFFFFF	ColorKeyAND4	Defines a 24-bit Mask where the pixel is ANDed before it's keyed with the COLORKEY value.
Offset 0x10 E184			*Color Key Up4*	
31:24		-	Unused	
23:0	R/W	0	ColorKeyup4	Defines a 24-bit color key used for color keying inside the layer.
Offset 0x10 E188			*Color Key Low4*	
31:24		-	Unused	
23:0	R/W	0	ColorKeylow4	Defines a 24-bit color key used for color keying inside the layer.
Offset 0x10 E18C			*Color Key Replace4*	
31	R/W	0	Colorkeyreplaceen	Enables color replacement.
30:24		-	Unused	
23:0	R/W	0	ColorKeyreplace4	Defines a 24-bit color to be put into the data path if the color key matches.
Offset 0x10 E190			*Color Key Mask/ROP*	
31:28		-	Unused	

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ADVANCED IMAGE COMPOSITION PROCESSOR 1 (AICP) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
27:24	R/W	0x0	KeyFwd Note: This function is not implemented in PNX8526	These bits can revert the results of the ColorKeyPassROP for the individual 4 color keys of a layer. The results are 4 individual decision signals: KeyFwd[0] XOR ColorKeyPassROP KeyFwd[1] XOR ColorKeyPassROP KeyFwd[2] XOR ColorKeyPassROP KeyFwd[3] XOR ColorKeyPassROP 0= Select previous pixel color key. 1= Select new pixel color key n.
23:20	R/W	0	ColorKeyMask	This mask specifies which color to key in for the current pixel coming out of the layer.
19:16	R/W	0	ColorKeyMaskP	This color Mask is used to decide which color key to use for the incoming previous pixel.
15:8	R/W	0	PassZeroROP	This ROP decides if the output key value is 0 or is the one selected by ColorKeyPassROP. 1 = No color key (4-bit vector is 0). 0 = Color key vector selected by ColorKeyPassROP.
7:0	R/W	0	ColorKeyPassROP	This ROP determines which color key to select for the current mixer output. ROP output: 1= Select previous pixel color key. 0= Select new pixel color key.
Offset 0x10 E194			*Pixel Invert/Select ROP*	
31:16	R/W	0	InvertROP	This ROP decides if the previous pixel is inverted or not. ROP output: 1 = Invert previous pixel. 0 = Do not invert previous pixel.
15:0	R/W	0	SelectROP	This ROP determines which pixel to select for the current mixer output. ROP output: 1 = Select previous pixel. 0 = Select new pixel.
Offset 0x10 E198			*Alpha Blend/Key Pass*	
31:16	R/W	0	AlphaBlend	This ROP value determines whether or not to do an alpha blend. ROP output: 1 = Do alpha-blending. 0 = No alpha-blending
15:0	R/W	0	KeyPass	This ROP generates the key which is passed to the next layer mixer and is used as KEY0 in those ROPs.
Offset 0x10 E19C			*Alpha Pass*	
31:16	R/W	0	AlphaPass	This ROP value determines which alpha is passed to the next mixer stage. ROP output: 1 = Alpha of previous pixel 0 = Alpha of current pixel
15:0		-	Unused	
Offset 0x10 E1A0			*Color Key ROPs 1/2*	
31:16		-	Unused	
15:8	R/W	0	ColorKeyROP1	This ROP determines if results of component color keying are true or not. Keys to the ROP are range_match upper, middle, lower. Upper match is key2, middle match is key1, lower match is key0. 0 = Color key didn't match. 1 = Color key matched.

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ADVANCED IMAGE COMPOSITION PROCESSOR 1 (AICP) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
7:0	R/W	0	ColorKeyROP2	This ROP determines if results of component color keying are true or not. Keys to the ROP are range_match upper, middle, lower. Upper match is key2, middle match is key1, lower match is key0. 0 = Color key didn't match. 1 = Color key matched.
Offset 0x10 E1A4			*Color Key ROPs 3/4*	
31:16		-	Unused	
15:8	R/W	0	ColorKeyROP3	This ROP determines if results of component color keying are true or not. Keys to the ROP are range_match upper, middle, lower. Upper match is key2, middle match is key1, lower match is key0. 0 = Color key didn't match. 1 = Color key matched.
7:0	R/W	0	ColorKeyROP4	This ROP determines if the results of component color keying are true or not. Keys to the ROP are range_match upper, middle, lower. Upper match is key2, middle match is key1, lower match is key0. 0 = Color key didn't match. 1 = Color key matched.
Offset 0x10 E1A8			*Matrix Coefficients1*	
31:26		-	Unused	
25:16	R/W	0	CSCa12	2. cs matrix coefficient
15:10		-	Unused	
9:0	R/W	0x100	CSCa11	1. cs matrix coefficient
Offset 0x10 E1AC			*Matrix Coefficients2*	
31:26		-	Unused	
25:16	R/W	0	CSCa21	4. cs matrix coefficient
15:10		-	Unused	
9:0	R/W	0	CSCa13	3. cs matrix coefficient
Offset 0x10 E1B0			*Matrix Coefficients3*	
31:26		-	Unused	
25:16	R/W	0	CSCa23	6. cs matrix coefficient
15:10		-	Unused	
9:0	R/W	0x100	CSCa22	5. cs matrix coefficient
Offset 0x10 E1B4			*Matrix Coefficients4*	
31:26		-	Unused	
25:16	R/W	0	CSCa32	8. cs matrix coefficient
15:10		-	Unused	
9:0	R/W	0	CSCa31	7. cs matrix coefficient
Offset 0x10 E1B8			*Matrix Coefficients5*	
31:22	R/W	-	Unused	
21	R/W	0	TC_out3	Lower output two's complement switch 1 = Two's complement data 0 = Binary data

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ADVANCED IMAGE COMPOSITION PROCESSOR 1 (AICP) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
20	R/W	0	TC_out2	Middle output two's complement switch 1 = Two's complement data 0 = Binary data
19	R/W	0	TC_out1	Upper output two's complement switch 1 = Two's complement data 0 = Binary data
18	R/W	0	TC3	Lower input two's complement switch 1 = Two's complement data 0 = Binary data
17	R/W	0	TC2	Middle input two's complement switch 1 = Two's complement data 0 = Binary data
16	R/W	0	TC1	Upper input two's complement switch 1 = Two's complement data 0 = Binary data
15:10		-	Unused	
9:0	R/W	0x100	CSCa33	9. cs matrix coefficient
Offset 0x10 E1BC			*DC-Offsets CSM Output*	
31:24		-	Unused	
23:16	R/W	0x0	Offset3	DC-offset lower output channel 8-bit two's complement
15:8	R/W	0x0	Offset2	DC-offset middle output channel 8-bit two's complement
7:0	R/W	0x0	Offset1	DC-offset upper output channel 8-bit two's complement
Offset 0x10 E1C0			*Layer Background Color*	
31	R/W	0	BG_enable	This bit enables the replacement of the previous input by the specified background color. 1 = Replace 0 = Use previous mixer output.
30:24		-	Unused	
23:16	R/W	0	Upper	Upper channel of the background color (R/Y)
15:8	R/W	0	Middle	Middle channel of the background color (G/U)
7:0	R/W	0	Lower	Lower channel of the background color (B/V)
Offset 0x10 E1C4			*DC-Offsets CSM Input*	
31		-	Unused	
23:16	R/W	0	Offset_in3	DC-offset lower input channel 8-bit two's complement
15:8	R/W	0	Offset_in2	DC-offset middle input channel 8-bit two's complement
7:0	R/W	0	Offset_in1	DC-offset upper input channel 8-bit two's complement
Offset 0x10 E1C8			*Start Fetch*	
31	R/W	0	Enable	This bit enables the start fetch functionality.
30:12	R/W	-	Unused	
11:0	R/W	0	Fetch Start	The current layer starts fetching data whenever the internal line counter reaches this point.

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ADVANCED IMAGE COMPOSITION PROCESSOR 1 (AICP) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 EFE0			*Interrupt Status AICP1*	
31:20	R	NI	y_positon	Current line position of the STG timing generator
19:16	R	NI	buffer status flags	Bit 16 corresponds to the current buffer status of layer4. Bit 17 corresponds to the current buffer status of layer3. Bit 18 corresponds to the current buffer status of layer2. Bit 19 corresponds to the current buffer status of layer1. 0 = buffer A 1 = buffer B
15	R	0	end_layer1_int	This bit is set when an end of layer 1 interrupt occurs.
14	R	0	end_layer2_int	This bit is set when an end of layer 2 interrupt occurs.
13	R	0	end_layer3_int	This bit is set when an end of layer 3 interrupt occurs. Unused in AICP2.
12	R	0	end_layer4_int	This bit is set when an end of layer 4 interrupt occurs. Unused in AICP2.
11	R	0	fifo_underflow1_int	This bit is set when a FIFO underflow in layer 1 occurs.
10	R	0	fifo_underflow2_int	This bit is set when a FIFO underflow in layer 2 occurs.
9	R	0	fifo_underflow3_int	Bit is set when a FIFO underflow in layer 3 occurs. Unused in AICP2.
8	R	0	fifo_underflow4_int	Bit is set when a FIFO underflow in layer 4 occurs. Unused in AICP2.
7	R	0	vlinta	This bit is set when the VLINTA specified in vinterrupt register occurs.
6	R	0	vlintb	This bit is set when the VLINTB specified in vinterrupt register occurs.
5	R	0	buffer_reuse_layer1_int	This bit is set when a buffer reuse interrupt for layer 1 occurs.
4	R	0	buffer_reuse_layer2_int	This bit is set when a buffer reuse interrupt for layer 2 occurs.
3	R	0	buffer_reuse_layer3_int	This bit is set, when a buffer reuse interrupt for layer 3 occurs. Unused in AICP2.
2	R	0	buffer_reuse_layer4_int	This bit is set when a buffer reuse interrupt for layer 4 occurs. Unused in AICP2.
1	R	0	vbi_done_int	This bit is set when a VBI done interrupt occurs. All VBI packets are transferred.
0	R	0	vbi_packet_int	This bit is set when a VBI packet is specified to issue an interrupt.
Offset 0x10 EFE4			*Interrupt Enable AICP1*	
31:16		-	Unused	
15:0	R/W	0	Interrupt Enables	A ‘1’ in the appropriate bit will enable the interrupt according to the specification in register 0xFE0.
Offset 0x10 EFE8			*Interrupt Clear AICP1*	
31:16		-	Unused	
15:0	W	0	Interrupt Clears	A ‘1’ in the appropriate bit will clear the interrupt according to the specification in register FE0.
Offset 0x10 EFEC			*Interrupt Set AICP1*	
31:16		-	Unused	
15:0	W	0	Interrupt Sets	A ‘1’ in the appropriate bit will set the interrupt according to the specification in register FE0.

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ADVANCED IMAGE COMPOSITION PROCESSOR 1 (AICP) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x10 EFF4			*Powerdown*	
31	R/W	0	Powerdown	This bit has no effect i.e., there is no powerdown implemented for this module.
30:0		-	Unused	
Offset 0x10 EFFC			*Module ID*	
31:16	R	0x0111A ICP1 0x0118 AICP2	Module ID	Unique revision number
15:12	R	1	REV_MAJOR	Major revision counter
11:8	R	0	REV_MINOR	Minor revision counter
7:0	R	0	APP_SIZE	Aperture Size 0 = 4 kB

AICP 2 Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.28)

ADVANCED IMAGE COMPOSITION PROCESSOR 2 (AICP) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
The AICP 2 registers begin at offset 0x10 F000 and correspond to the AICP 1 registers, with the following exceptions: - AICP 2 does not support Output gamma LUT control. (Registers 0x10 F040-F04C are reserved.) - AICP 2 supports only two layers. (Registers 0x10 F300-FFD8 are reserved.) - Because of these differences, note the settings in the Features register.				
Offset 0x10 F018			*FEATURES*	
31:5		-	Unused	
4:3	R	0x0	NOGAMMALUTS	Number of gamma LUTS binary coded for the output channels (The first slice of the AICP out goes through the gamma LUT.): Value for AICP2 is 0x0.
2:0	R	0x2	NOLAYERS	Number of layers in this AICP: Value for AICP2 is 0x2.
Note: For the interrupt to occur, it must be enabled in the STG control register.				
Offset 0x10 FFE0			*Interrupt Status AICP2*	
31:20	R		y_position	Current line position of the STG timing generator
19:18		-	Unused	
17:16	R		buffer status flags	Bit 17 corresponds to the current buffer status of layer1. Bit 16 corresponds to the current buffer status of layer2.
15	R	0	end_layer1_int	This bit is set when an end of layer 1 interrupt occurs.
14	R	0	end_layer2_int	This bit is set when an end of layer 2interrupt occurs.
13		-	Unused	
12		-	Unused	
11	R	0	fifo_underflow1_int	This bit is set, when a fifo underflow in layer 1 occurred
10	R	0	fifo_underflow2_int	This bit is set, when a fifo underflow in layer 2 occurred

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ADVANCED IMAGE COMPOSITION PROCESSOR 2 (AICP) REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
9		-	Unused	
8		-	Unused	
7	R	0	vlinta	This bit is set when the vertical line interrupt a specified in vinterrupt register occurs.
6	R	0	vlintb	This bit is set when the vertical line interrupt b specified in vinterrupt register occurs.
5	R	0	buffer_reuse_layer1_int	This bit is set when a buffer reuse interrupt for layer 1 occurs.
4	R	0	buffer_reuse_layer2_int	This bit is set when a buffer reuse interrupt for layer 2 occurs.
3		-	Unused	
2		-	Unused	
1	R	0	vbi_done_int	This bit is set when a VBI done interrupt occurs. All VBI packets are transferred.
0	R	0	vbi_packet_int	This bit is set when a VBI packet is specified to issue an interrupt

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Audio I2S Output Ports 1 Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.21)

AUDIO (I2S) OUTPUT PORTS 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Audio Out 1 Registers (Offset 0x11 0000), Audio Out 2 Registers (Offset 0x11 2000) and Audio Out 3 Registers (Offset 0x11 4000) The Audio Out 1, 2 and 3 registers are identical except for their offsets. A triplicate set has been created to facilitate programming. The tables for Audio Out 2 (0x11 2000) and 3 (0x11 4000) registers follow this table.				
Note: The clock frequency emitted by the OSCLK output can be found in *PNX8526 User Manual, Ref. UM10104_1*, at Offset 0x04 7314 AO1_OSCLK_CTL.				
Offset 0x11 0000			*AO_STATUS*	
31:6		-	Unused	
5	R	0	CC_BUSY	0 = Audio Out is ready to receive a CC1, CC2 pair. 1 = Audio Out is not ready to receive a CC1, CC2 pair. Try again in a few SCK clock intervals.
4	R	1	BUF1_ACTIVE	1 = buffer 1 will be used for the next sample to be transmitted. 0 = buffer 2 will contain the next sample.
3	R	0	UNDERRUN	An UNDERRUN error has occurred i.e., the system controller/software failed to provide a full buffer in time and no samples were transmitted, although requested by the D/A converter. If UDR_INTEN is also 1, an interrupt request is pending. The UNDERRUN flag can ONLY be cleared by writing a '1' to ACK_UDR.
2	R	0	HBE	Bandwidth Error indicates that no data was transmitted due to an inability to read the local AO buffer from memory in time.
1	R	0	BUF2_EMPTY	If 1, buffer 2 is empty. If BUF2_INTEN is also 1, an interrupt request is asserted. BUF2_EMPTY is cleared by writing a '1' to ACK2, at which point the Audio Out hardware will assume that AO_BASE2 and AO_SIZE describe a new full buffer.
0	R	0	BUF1_EMPTY	If 1, buffer 1 is empty. If BUF1_INTEN is also 1, an interrupt request is asserted. BUF1_EMPTY is cleared by writing a '1' to ACK1, at which point the Audio Out hardware will assume that AO_BASE1 and AO_SIZE describe a new full buffer.
Offset 0x11 0004			*AO_CTL*	
31	R/W	0	RESET	Resets the Audio Out logic. See *PNX8526 User Manual, Ref. UM10104_1*, Chapter 21 for a description of the recommended procedure.
30	R/W	0	TRANS_ENABLE	Transmission Enable flag 0 = Audio Out is inactive. 1 = Audio Out transmits samples and acts as DMA master to read samples from local memory. Do not change the POLARITY bit while transmission is enabled.

AUDIO (I2S) OUTPUT PORTS 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
29:28	R/W	00	TRANS_MODE	00 = Mono, 32 bits/sample. Left and right data sent to each active output are the same. 01 = Stereo, 32 bits/sample 10 = Mono, 16 bits/sample. Left and right data are the same. 11 = Stereo, 16 bits/sample
27	R/W	0	SIGN_CONVERT	0 =Leave msb unchanged. 1 = Invert msb (not applied to codec control fields).
26:25		-	Unused	
24	R/W	0	CC1_EN	0 = CC1 emission disabled. 1 = CC1 emission enabled.
23	R/W	0	CC2_EN	0 = CC2 emission disabled. 1 = CC2 emission enabled.
22	R/W	0	WS_PULSE	0 = Emit 50% AO_WS. 1 = Emit single AO_SCK cycle AO_WS.
21:8		-	Unused	
7	R/W	0	UDR_INTEN	UNDERRUN Interrupt Enable. 0 = No interrupt 1 = Interrupt if an UNDERRUN error occurs.
6	R/W	0	HBE_INTEN	HBE Interrupt Enable: 0 = No interrupt 1 = Interrupt if a data bus bandwidth error occurs.
5	R/W	0	BUF2_INTEN	Buffer 2 Empty Interrupt Enable: 0 = No interrupt 1 = Interrupt if buffer 2 empty
4	R/W	0	BUF1_INTEN	Buffer 1 Empty Interrupt Enable: 0 = No interrupt 1 = Interrupt if buffer 1 empty.
3	R/W	0	ACK_UDR	Write a 1 to clear the UNDERRUN flag and remove any pending UNDERRUN interrupt request. ACK_UDR always reads 0.
2	R/W	0	ACK_HBE	Write a 1 to clear the HBE flag and remove any pending HBE interrupt request. ACK_HBE always reads as 0.
1	R/W	0	ACK2	Write a 1 to clear the BUF2_EMPTYflag and remove any pending BUF2_EMPTY interrupt request. ACK2 always reads 0.
0	R/W	0	ACK1	Write a 1 to clear the BUF1_EMPTY flag and remove any pending BUF1_EMPTY interrupt request. ACK1 always reads 0.
Offset 0x11 0008			*AO_SERIAL*	
31	R/W	0	SER_MASTER	0 = The D/A subsystem is the timing master over the Audio Out serial interface. SCK and WS act as inputs. 1 = AO is the timing master over serial interface. SCK and WS act as outputs. This mode is required for 4, 6 or 8 channel operation. The SER_MASTER bit should only be changed while Audio Out is disabled i.e. TRANS_ENABLE = 0.
30	R/W	0	DATAMODE	0 = msb first 1 = lsb first
29	R/W	0	CLOCK_EDGE	0 = The parallel-to-serial converter samples WS on positive edges of SCK and outputs data on the negative edge of SCK. 1 = The parallel-to-serial converter samples WS on negative edges of SCK and outputs data on positive edges of SCK.
28:19		-	Unused	

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AUDIO (I2S) OUTPUT PORTS 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
18:17	R/W	00	NR_CHAN	00 = Only SD[0] is active. 01 = SD[0] and [1] are active. 10 = SD[0], [1], and [2] are active. 11 = SD[0]..SD[3] are active. Each SD output receives either 1 or 2 channels depending on TRANS_MODE. Non-active channels receive 0 value samples. In mono modes, each channel of a SD output receives identical left and right samples. Audio Out 1 and 2 have one data line which must be set to 00.
16:8	R/W	0x0	WSDIV	Sets the divider used to derive WS from SCK. Set to 0..511 for a serial frame length of 1..512.
7:0	R/W	0x0	SCKDIV	Sets the divider used to derive SCK from OSCLK. Set to 0..255 for division by 1..256.
Offset 0x11 000C			*AO_FRAMING*	
31	R/W	0	POLARITY	0 = Serial frame starts with a WS neg. edge 1 = Serial frame starts with a WS pos. edge This bit should not be changed during operation of Audio Out i.e., only update this bit when TRANS_ENABLE = 0.
30	R/W	0	SSPOS4	Start/Stop bit position msb. Note that SSPOS is a 5-bit field, while bit SSPOS4 is non-adjacent for backwards compatibility in 16-bit/sample modes. Program this field along with AO_FRAMING[3:0].
29:22		-	Unused	
21:13	R/W	0x0	LEFTPOS	Defines the bit position within a serial frame where the first data bit of the left channel is placed.
12:4	R/W	0x0	RIGHTPOS	Defines the bit position within a serial frame where the first data bit of the right channel is placed.
3:0	R/W	0x0	SSPOS	Start/Stop bit position. Note that SSPOS is a 5-bit field, while bit SSPOS4 is non-adjacent for backwards compatibility in 16-bit/sample modes. Program this field along with AO_FRAMING[3:0]. If DATAMODE = msb first, transmission starts with the msb of the sample i.e., bit 15 for 16-bit/sample modes or bit 31 for 32-bit/sample modes. SSPOS determines the bit index (0..31) in the parallel input word of the last transmitted data bit. If DATAMODE = lsb first, SSPOS determines the bit index (0..31) in the parallel word of the first transmitted data bit. Bits SSPOS up to and including the msb are transmitted i.e., up to bit 15 in 16-bit/sample mode and bit 31 in 32-bit/sample mode.
Offset 0x11 0010			*Reserved*	
Offset 0x11 0014			*AO_BASE1*	
31:6	R/W	0x0	BASE1	Base Address of buffer1 must be a 64-byte aligned address in local memory.
5:0		-	Unused	
Offset 0x11 0018			*AO_BASE2*	
31:6	R/W	0x0	BASE2	Base Address of buffer2 must be a 64-byte aligned address in local memory.
5:0		-	Unused	
Offset 0x11 001C			*AO_SIZE*	

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AUDIO (I2S) OUTPUT PORTS 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
31:6	R/W	0	SIZE	DMA buffer size in samples. The number of mono samples or stereo sample pairs is read from a DMA buffer before switching to the other buffer. Buffer size in bytes is as follows: 16 bps, mono: 2 * SIZE 32 bps, mono: 4 * SIZE 16 bps, stereo: 4 * SIZE 32 bps, stereo: 8 * SIZE
5:0		-	Unused	
Offset 0x11 0020			*AO_CC*	
31:16	R/W	0x0	CC1	The 16-bit value of CC1 is shifted into each emitted serial frame starting at bit position CC1_POS, as long as CC1_EN is asserted.
15:0	R/W	0x0	CC2	The 16-bit value of CC2 is shifted into each emitted serial frame starting at bit position CC2_POS, as long as CC2_EN is asserted.
Offset 0x11 0024			*AO_CFC*	
31:18		-	Unused	
17:10	R/W	0x0	CC1_POS	Defines the bit position within a serial frame where the first data bit of CC1 is placed.
9:0	R/W	0x0	CC2_POS	Defines the bit position within a serial frame where the first data bit of CC2 is placed.
Offset 0x11 0028—0FF0			*Reserved*	

AUDIO (I2S) OUTPUT PORTS 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x11 0FF4			*AO_PWR_DWN*	
31:1		-	Unused	
0	R/W	0	PWR_DWN	The bit is used to provide power control status for system software block power management.
Offset 0x11 0FFC			*AO_MODULE_ID*	
31:16	R	0x0120	ID	Module ID. This field identifies the block as type Audio Out.
15:12	R	0	MAJ_REV	Major Revision ID. This field is incremented by 1 when changes introduced in the block result in software incompatibility with the previous version of the block. First version default = 0.
11:8	R	0	MIN_REV	Minor Revision ID. This field is incremented by 1 when changes introduced in the block result in software *compatibility* with the previous version of the block. First version default = 0.
7:0	R	0	APERTURE	Aperture size. Identifies the MMIO aperture size in units of 4 kB for the AO block. AO has an MMIO aperture size of 4 kB. Aperture = 0: 4 kB.

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Audio I2S Input Ports 1 Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.20)

AUDIO (I2S) INPUT PORTS 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Audio In 1 Registers (Offset 0x11 1000), Audio In 2 Registers (Offset 0x11 3000) and Audio In 3 Registers (Offset 0x11 5000) The Audio In 1, 2 and 3 registers are identical except for their offsets. A triplicate set has been created to facilitate programming. The tables for Audio In 2 (0x11 3000) and 3 (0x11 5000) registers follow this table.				
Note: The clock frequency emitted by the AI_OSCLK output is set at Offset 0x04 7310 AI1_OSCLK_CTL. See *PNX8526 User Manual, Ref. UM10104_1, Chapter 5*.				
Offset 0x11 1000			*AI_STATUS*	
31:5		-	Unused	
4	R	1	BUF1_ACTIVE	1 = Buffer will be used for the next incoming sample. 0 = Buffer 2 will receive the next sample.
3	R	0	OVERRUN	An OVERRUN error has occurred i.e., software failed to provide an empty buffer in time and 1 or more samples have been lost.
2	R	0	HBE	Bandwidth Error
1	R	0	BUF2_FULL	1 = Buffer 2 is full. If BUF2_INTEN is also 1, an interrupt request is pending.
0	R	0	BUF1_FULL	1 = Buffer 1 is full. If BUF1_INTEN is also 1, an interrupt request is pending.
Offset 0x11 1004			*AI_CTL*	
31	R/W	0	RESET	The Audio In logic is reset by writing a 0x80000000 to AI_CTL. This bit always reads as a '0'.
30	R/W	0	CAP_ENABLE	Capture Enable flag: 0 = Audio In is inactive. 1 = Audio In captures samples and acts as DMA master to write samples to local memory.
29:28	R/W	00	CAP_MODE	00 = Mono (left ADC only), 8 bits/sample 01 = Stereo, 2 times 8 bits/sample 10 = Mono (left ADC only), 16 bits/sample 11 = Stereo, 2 times 16 bits/sample
27	R/W	0	SIGN_CONVERT	0 = Leave msb unchanged. 1 = Invert msb.
26		-	Unused	
25	R/W	0	DIAGMODE	0 = Normal operation 1 = Diagnostic mode
24:8		-	Unused	
7	R/W	0	OVR_INTEN	Overrun Interrupt Enable: 0 = No interrupt 1 = Interrupt if an overrun error occurs.
6	R/W	0	HBE_INTEN	HBE Interrupt Enable: 0 = No interrupt 1 = Interrupt if a bandwidth error occurs.
5	R/W	0	BUF2_INTEN	Buffer 2 full interrupt Enable: 0 = No interrupt 1 = Interrupt if buffer 2 full.
4	R/W	0	BUF1_INTEN	Buffer 1 full Interrupt Enable: 0 = No interrupt 1 = Interrupt if buffer 1 full.

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AUDIO (I2S) INPUT PORTS 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
3	R/W	0	ACK_OVR	Write a 1 to clear the OVERRUN flag and remove any pending OVERRUN interrupt request. This bit always reads as 0.
2	R/W	0	ACK_HBE	Write a 1 to clear the HBE flag and remove any pending HBE interrupt request. This bit always reads as 0.
1	R/W	0	ACK2	Write a 1 to clear the BUF2_FULL flag and remove any pending BUF2_FULL interrupt request. This bit always reads as 0.
0	R/W	0	ACK1	Write a 1 to clear the BUF1_FULL flag and remove any pending BUF1_FULL interrupt request. This bit always reads as 0.
Offset 0x11 1008			*AI_SERIAL*	
31	R/W	0	SER_MASTER	Sets clock ratios and internal/external clock generation. 0 = The A/D converter is the timing master over the serial interface. AI_SCK and AI_WS pins are set to be input. 1 = Audio In serial interface is the timing master over the external A/D. The AI_SCK and AI_WS pins are set to be outputs.
30	R/W	0	DATAMODE	0 = msb first 1 = lsb first
29:28	R/W	00	FRAMEMODE	This mode governs capturing of samples. 00 = Accept a sample every serial frame. 01 = Unused, reserved 10 = Accept sample if valid bit = 0. 11 = Accept sample if valid bit = 1.
27	R/W	0	CLOCK_EDGE	0 = The SD and WS pins are sampled on positive edges of the SCK pin. If SER_MASTER = 1, WS is asserted on SCK negative edge. 1 = SD and WS are sampled on negative edges of SCK. As output, WS is asserted on SCK positive edge.
26:17		-	Unused	
16:8	R/W	0	WSDIV	Sets the divider used to derive AI_WS from AI_SCK. Set to 0..511 for a serial frame length of 1..512.
7:0	R/W	0	SCKDIV	Sets the divider used to derive AI_SCK from AI_OSCLK. Set to 0..255, for division by 1..256.
Offset 0x11 100C			*AI_FRAMING*	
31	R/W	0	POLARITY	Sets format of serial data stream. 0 = Serial frame starts on WS negative edge. 1 = Serial frame starts on WS positive edge.
29:22	R/W	0	VALIDPOS	Defines bit position within a serial frame where the valid bit is found.
21:13	R/W	0	LEFTPOS	Defines bit position within a serial frame where the first data bit of the left channel is found.
12:4	R/W	0	RIGHTPOS	Defines bit position within a serial frame where the first data bit of the right channel is found.
3:0	R/W	0	SSPOS	Start/Stop bit position. If DATAMODE = msb first, SSPOS determines the bit index (0..15) in the parallel word of the *last* data bit. Bits 15 (msb) up to and including SSPOS are taken in order from the serial frame data. All other bits are set to zero. If DATAMODE = lsb first, SSPOS determines the bit index (0..15) in the parallel word of the first data bit. Bits SSPOS up to and including 15 are taken in order from the serial frame data. All other bits are set to zero.
Offset 0x11 1010			*Reserved*	

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AUDIO (I2S) INPUT PORTS 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x11 1014			*AI_BASE1*	
31:6	R/W	0	BASE1	Base Address of buffer 1 must be a 64-byte aligned address in local memory.
5:0			Reserved	
Offset 0x11 1018			*AI_BASE2*	
31:6	R/W	0	BASE2	Base Address of buffer 1 must be a 64-byte aligned address in local memory.
5:0			Reserved	
Offset 0x11 101C			*AI_SIZE*	
31:6	R/W	0	SIZE	Sets number of samples in buffers before switching to other buffers. In stereo modes, a pair of 8-bit or 16-bit data counts as 1 sample. In mono modes, a single value counts as a sample.
5:0			Reserved	
Offset 0x11 1020—1FF0			*Reserved*	

AUDIO (I2S) INPUT PORTS 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x11 1FF4			*AI_PWR_DWN*	
31:1		-	Unused	
0	R/W	0	PWR_DWN	The bit is used to provide power control status for system software block power management. Not implemented.
Offset 0x11 1FFC			*AI_MODULE_ID*	
31:16	R	0x010D	ID	Module ID. This field identifies the block as type Audio In.
15:12	R	0	MAJ_REV	Major Revision ID. This field is incremented by 1 when changes introduced in the block result in software incompatibility with the previous version of the block. First version default = 0.
11:8	R	0	MIN_REV	Minor Revision ID. This field is incremented by 1 when changes introduced in the block result in software compatibility with the previous version of the block. First version default = 0.
7:0	R	0	APERTURE	Aperture size. Identifies the MMIO aperture size in units of 4 kB for the AI block. AI has an MMIO aperture size of 4 kB. Aperture = 0: 4 kB.

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Audio I2S Output Ports 2 Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.21)

AUDIO (I2S) OUTPUT PORTS 2 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Audio Out 1 Registers (Offset 0x11 0000), Audio Out 2 Registers (Offset 0x11 2000) and Audio Out 3 Registers (Offset 0x11 4000) The Audio Out 1, 2 and 3 registers are identical except for their offsets. A triplicate set has been created to facilitate programming. The tables for Audio Out 1 (0x11 0000) and 3 (0x11 4000) registers precede and follow this table respectively.				
Note: The clock frequency emitted by the AO_OSCLK output can be found in *PNX8526 User Manual, Ref. UM10104_1, Chapter 5*, at Offset 0x04 731C AO2_OSCLK_CTL				
Offset 0x11 2000			*AO_STATUS*	
Offset 0x11 2004			*AO_CTL*	
Offset 0x11 2008			*AO_SERIAL*	
Offset 0x11 200C			*AO_FRAMING*	
Offset 0x11 2010			*Reserved*	
Offset 0x11 2014			*AO_BASE1*	
Offset 0x11 2018			*AO_BASE2*	
Offset 0x11 201C			*AO_SIZE*	
Offset 0x11 2020			*AO_CC*	
Offset 0x11 2024			*AO_CFC*	
Offset 0x11 2028—2FF0			*Reserved*	
Offset 0x11 2FF4			*AO_PWR_DWN*	
Offset 0x11 2FFC			*AO_MODULE_ID*	

Audio I2S Input Ports 2 Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.20)

AUDIO (I2S) INPUT PORTS 2 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Audio In 1 Registers (Offset 0x11 1000), Audio In 2 Registers (Offset 0x11 3000) and Audio In 3 Registers (Offset 0x11 5000) The Audio In 1, 2 and 3 registers are identical except for their offsets. A triplicate set has been created to facilitate programming. The tables for Audio In 1 (0x11 1000) and 3 (0x11 5000) registers precede and follow this table respectively.				
Note: The clock frequency emitted by the AI_OSCLK output can be found in *PNX8526 User Manual, Ref. UM10104_1, Chapter 5* at Offset 0x04 7318 AI2_OSCLK_CTL				
Offset 0x11 3000			*AI_STATUS*	
Offset 0x11 3004			*AI_CTL*	
Offset 0x11 3008			*AI_SERIAL*	
Offset 0x11 300C			*AI_FRAMING*	
Offset 0x11 3010			*Reserved*	
Offset 0x11 3014			*AI_BASE1*	
Offset 0x11 3018			*AI_BASE2*	
Offset 0x11 301C			*AI_SIZE*	

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AUDIO (I2S) INPUT PORTS 2 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x11 3020—3FF0			*Reserved*	
Offset 0x11 3FF4			*AI_PWR_DWN*	
Offset 0x11 3FFC			*AI_MODULE_ID*	

Audio I2S Output Ports 3 Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.21)

AUDIO (I2S) OUTPUT PORTS 3 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Audio Out 1 Registers (Offset 0x11 0000), Audio Out 2 Registers (Offset 0x11 2000) and Audio Out 3 Registers (Offset 0x11 4000) The Audio Out 1, 2 and 3 registers are identical except for their offsets. A triplicate set has been created to facilitate programming. The tables for Audio Out 1 (0x11 0000) and 2 (0x11 2000) registers precede this table.				
Note: The clock frequency emitted by the AO_OSCLK output can be found in *PNX8526 User Manual, Ref. UM10104_1, Chapter 5,* at Offset 0x04 7320 AO3_OSCLK_CTL				
Offset 0x11 4000			*AO_STATUS*	
Offset 0x11 4004			*AO_CTL*	
Offset 0x11 4008			*AO_SERIAL*	
Offset 0x11 400C			*AO_FRAMING*	
Offset 0x11 4010			*Reserved*	
Offset 0x11 4014			*AO_BASE1*	
Offset 0x11 4018			*AO_BASE2*	
Offset 0x11 401C			*AO_SIZE*	
Offset 0x11 4020			*AO_CC*	
Offset 0x11 4024			*AO_CFC*	
Offset 0x11 4028—4FF0			*Reserved*	
Offset 0x11 4FF4			*AO_PWR_DWN*	
Offset 0x11 4FFC			*AO_MODULE_ID*	

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Audio I2S Input Ports 3 Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.20)

AUDIO (I2S) INPUT PORTS 3 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Audio In 1 Registers (Offset 0x11 1000), Audio In 2 Registers (Offset 0x11 3000) and Audio In 3 Registers (Offset 0x11 5000) The Audio In 1, 2 and 3 registers are identical except for their offsets. A triplicate set has been created to facilitate programming. The tables for Audio In 1 (0x11 1000) and 2 (0x11 3000) registers precede this table.				
Note: The clock frequency emitted by the AI_OSCLK output can be found in *PNX8526 User Manual, Ref. UM10104_1, Chapter 5* at Offset 0x04 7320 AI3_OSCLK_CTL				
Offset 0x11 5000			*AI_STATUS*	
Offset 0x11 5004			*AI_CTL*	
Offset 0x11 5008			*AI_SERIAL*	
Offset 0x11 500C			*AI_FRAMING*	
Offset 0x11 5010			*Reserved*	
Offset 0x11 5014			*AI_BASE1*	
Offset 0x11 5018			*AI_BASE2*	
Offset 0x11 501C			*AI_SIZE*	
Offset 0x11 5020—5FF0			*Reserved*	
Offset 0x11 5FF4			*AI_PWR_DWN*	
Offset 0x11 5FFC			*AI_MODULE_ID*	

TSDMA Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.31)

SOFTWARE TRANSPORT STREAM (TSDMA) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x11 6000			*TSDMA_CTRL*	
31:18		-	Unused	Read returns 00.
17	R/W	0	tsdma_eop2_en	Enable to route the eop signal to the tx2 interface (of the TS Network).
16	R/W	0	tsdma_eop1_en	Enable to route the eop signal to the tx1 interface (of the TS Network).
15:14		-	Unused	Read returns 00.
13	R/W	0	tsdma_header2_dis	Disables use of the header structure for DMA 2.
12	R/W	0	tsdma_header1_dis	Disables use of the header structure for DMA 1.
11:10		-	Unused	Read returns 00.
9	R/W	0	TSDMA2_SEND_ERROR_PACKETS	0 = Erroneous packets are not sent. 1 = Erroneous packets are sent. Using the error bit (bit 31 in the HEADER), the packet is evaluated if it is valid or not. If this bit is '1' the erroneous packets are sent like other packets setting the error signal. If this bit is '0' erroneous packets are discarded. Default = Erroneous packets are not sent. This bit has no meaning in non-header mode.

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SOFTWARE TRANSPORT STREAM (TSDMA) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
8	R/W	0	TSDMA1_SEND_ERROR_PACKETS	0 = Erroneous packets are not sent. 1 = Erroneous packets are sent. Using the error bit (bit 31 in the HEADER) the packet is evaluated if it is valid or not. If this bit is '1' the erroneous packets are sent like other packets setting the error signal. If this bit is '0' erroneous packets are discarded. Default = Erroneous packets are not sent. This bit has no meaning in non-header mode.
7:5		-	Unused	Read returns 00.
4	R/W	0	DMA loop	0 = No looping 1 = Looping Setting this bit will force the TSDMA to automatically restart a DMA channel. If DMA1 and DMA2 are enabled, looping will jump from DMA1 to DMA2, then back to DMA1 and so forth. If only DMA1 or DMA2 is enabled, looping will start with the enabled DMA again after it is done. If looping is disabled and DMA1 and DMA2 are enabled, first DMA1 will be finished, then DMA2, and then the TSDMA stops (unless DMA_END event was cleared by software). If looping is disabled and either DMA1 or DMA2 is enabled, the enabled DMA channel will be finished and then TSDMA stops (unless DMA_END event was cleared by software). Default = No looping.
3:2		-	Unused	Read returns 00s
1	R/W	0	TSDMA2_ENABLE	0 = Disable 1 = Enable This bit enables the DMA channel 2. The DMA controller should be enabled after all other settings are done for this channel. Default = Disable.
0	R/W	0	TSDMA1_ENABLE	0 = Disable 1 = Enable This bit enables the DMA channel 1. The DMA controller should be enabled after all other settings are done for this channel. Default = Disable.
TSDMA Read Channel 1 Setup				
Offset 0x11 6004			*TSDMA1_START_ADDRESS*	
31:2		0	TSDMA1_START_ ADDRESS	Start address for the DMA read buffer for DMA channel 1.
1:0		-	Unused	Read returns 00.
Offset 0x11 6008			*TSDMA1_PACKET_LENGTH*	
31:11		-	Unused	Read returns 00.
10:0	R/W	0	TSDMA1_PACKET_ LENGTH	This register defines the length of one packet in bytes. The specified length does not include the HEADER or padding bytes. The maximum packet length is 2047 bytes = 0x1FF.
Offset 0x11 600C			*TSDMA1_SIZE*	
31:18		-	Unused	Read returns 00.
17:0	R/W	0	TSDMA1_SIZE	TSDMA1_SIZE register defines size of the DMA buffer in 32-bit words. DMA_SIZE =[(PACKET_LENGTH + HEADER + PADDING BYTES) * Number of Packets]/4 with HEADER being 4 in header mode and 0 in non-header mode
Offset 0x11 6010			*TSDMA1_THRESHOLD*	
31:18		-	Unused	Read returns 00.

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SOFTWARE TRANSPORT STREAM (TSDMA) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
17:0	R/W	0	TSDMA1_THRESHOLD	The threshold is the number of 32-bit words which must remain unsent when the threshold flag is raised.
Offset 0x11 6014			*TSDMA1_DELIVERY OFFSET*	
31:0	R/W	0	TSDMA1_DELIVERY_ OFF-SET	In header mode: delivery offset is added to the timestamp of the packet structure for delivery schedule. In non-header mode: delivery offset is used as a delay for the delivery of the next packet.
TSDMA Read Channel 2 Setup				
Offset 0x11 6018			*TSDMA2_START_ADDRESS*	
31:2	R/W	0	TSDMA2_START_ADDRESS	Same as for TSDMA1
1:0		-	Unused	Read returns 00.
Offset 0x11 601C			*TSDMA2_PACKET_LENGTH*	
31:11		-	Unused	Read returns 00.
10:0	R/W	0	TSDMA2_PACKET_ LENGTH	Same as for TSDMA1
Offset 0x11 6020			*TSDMA2_SIZE*	
31:18		-	Unused	Read returns 00.
17:0	R/W	0	TSDMA2_SIZE	Same as for TSDMA1
Offset 0x11 6024			*TSDMA2_THRESHOLD*	
31:18		-	Unused	Read returns 00.
17:0	R/W	0	TSDMA2_THRESHOLD	Same as for TSDMA1
Offset 0x11 6028			*TSDMA2_DELIVERY_OFFSET*	
31:0	R/W	0	TSDMA2_DELIVERY_ OFF-SET	Same as for TSDMA1
Offset 0x11 602C			*TSDMA_TIMEOUT_VALUE*	
31:16		-	Unused	Read returns 00.
15:0	R/W	0	TSDMA_TIMEOUT_ VALUE	Relevant only in header mode. The TSDMA_TIMEOUT_VALUE is used to check if a packet is sent within a certain time after evaluating its timestamp. While the TSDMA module evaluates the timestamp to schedule the delivery of the packet, a timeout counter is running. The value of this counter is compared against this TSDMA_TIMEOUT_VALUE. If a packet is not sent after the counter reaches TSDMA_TIMEOUT_VALUE, a time-out flag is raised. The duration of the timeout is defined by the following equation: timeout-time =TSDMA_TIMEOUT_VALUE * 1/TSTAMP_clk. The TSTAMP_clk is the clock frequency set in the clocks module. Refer to *PNX8526 User Manual, Ref. UM10104_1, Chapter 31.*
Offset 0x11 6030			*TSDMA_TSTAMP_SEL*	
31:19		-	Unused	Read returns 00.

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SOFTWARE TRANSPORT STREAM (TSDMA) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
18:16	R/W	0	TSDMA_TSTAMP_SEL2	Selects the source of the signal to be timestamped in the GPIO module with TSDMA2: 0 = irx_fsync 1 = irx_sysync 2 = irx_seq_err 3 = irx_emi [0] 4 = irx_emi [1] 5 = tsdma_sync 6 = tsdma_last_byte 7 = wait Notes: All irx signals are outputs of the IEEE 1394 link core. The tsdma_last_byte signals the last byte of a packet being transferred. Wait is set when TSDMA is idling because it gets no data from the bus.
15:3		-	Unused	Read returns 00.
2:0	R/W	0	TSDMA_TSTAMP_SEL1	Selects the source of the signal to be timestamped in the GPIO module with TSDMA1: 0 = irx_fsync 1 = irx_sysync 2 = irx_seq_err 3 = irx_emi [0] 4 = irx_emi [1] 5 = tsdma_sync 6 = tsdma_last_byte 7 = wait Notes: All irx signals are outputs of the IEEE 1394 link core. The tsdma_last_byte signals the last byte of a packet being transferred. Wait is set when TSDMA is idling because it gets no data from the bus.
Offset 0x11 6034			*TSDMA_DMA_COUNT*	
31:18		-	Unused	
17:0	R	0	TSDMA_DMA_COUNT	This register gives the current value of the DMA COUNT. It only gives a stable value if the DMA is stopped.
Offset 0x11 6038—6FDC			*Reserved*	

SOFTWARE TRANSPORT STREAM (TSDMA) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x11 6FE0			*TSDMA_INT_STATUS*	
31:9		-	Unused	Returns 0.
8	R	0	TSDMA_ACTIVE	This flag indicates an active TSDMA.
7	R	0	TSDMA2_ACTIVE	This flag indicates an active channel DMA 2.
6	R	0	TSDMA1_ACTIVE	This flag indicates an active channel DMA 1.
5	R	0	TSDMA_STALL	Indicates the TSDMA is stalling because the system cannot deliver data (DMA read underflow).

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SOFTWARE TRANSPORT STREAM (TSDMA) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
4	R	0	TSDMA_TIMEOUT	This interrupt indicates the timeout condition as specified for the TSDMA_TIMEOUT_VALUE.
3	R	0	TSDMA2_THRES	This interrupt indicates that the DMA threshold is reached for channel2.
2	R	0	TSDMA1_THRES	This interrupt indicates that the DMA threshold is reached for channel1.
1	R	0	TSDMA2_END	This interrupt indicates the end of DMA channel 2.
0	R	0	TSDMA1_END	This interrupt indicates the end of DMA channel 1.
Offset 0x11 6FE4			*TSDMA_INT_EN*	
31:6		-	Unused	
5	R/W	0	TSDMA_STALL	Each of these bits enables generation of an interrupt by the appropriate bit in the TSDMA_INT_STATUS register.
4	R/W	0	TSDMA_TIMEOUT	
3	R/W	0	TSDMA2_THRES	
2	R/W	0	TSDMA1_THRES	
1	R/W	0	TSDMA2_END	
0	R/W	0	TSDMA1_END	
Offset 0x11 6FE8			*TSDMA_INT_CLR*	
31:6		-	Unused	
5	W	0	TSDMA_STALL	Each of these bits clears the interrupt bit in the status register TSDMA_INT_STATUS.
4	W	0	TSDMA_TIMEOUT	
3	W	0	TSDMA2_THRES	
2	W	0	TSDMA1_THRES	
1	W	0	TSDMA2_END	
0	W	0	TSDMA1_END	
Offset 0x11 6FEC			*TSDMA_INT_SET*	
31:6		-	Unused	
5	W	0	TSDMA_STALL	Each of these bits sets the interrupt bit in the status register TSDMA_INT_STATUS.
4	W	0	TSDMA_TIMEOUT	
3	W	0	TSDMA2_THRES	
2	W	0	TSDMA1_THRES	
1	W	0	TSDMA2_END	
0	W	0	TSDMA1_END	
Offset 0x11 6FF0			*Reserved*	
Offset 0x11 6FF4			*Power Down*	
31	R/W	0	Powerdown	TSDMA Powerdown indicator. 1 = Powerdown 0 = Power up When this bit equals 1, no other registers are accessible.
30:0		-	Unused	
Offset 0x11 6FF8			*Reserved*	

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SOFTWARE TRANSPORT STREAM (TSDMA) REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x11 6FFC			*TSDMA_MOD_ID*	
31:16	R	0x0125	TSDMA_MOD_ID	This is the module ID for the TSDMA module.
15:12	R	1	MAJREV	Major Revision
11:8	R	0	MINREV	Minor Revision
7:0	R	0	MODULE APERTURE SIZE	Encoded as: Aperture size = 4 k*(bit_value+1), so 0 means 4 kB (the default).

TPI Null 2 Module Registers

TPI NULL 2 MODULE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x11 7FFC			*Module ID Register*	
31:16	R	0x0124	MOD_ID	Module ID Number
15:12	R	0	REV_MAJOR	Major revision
11:8	R	0	REV_MINOR	Minor revision
7:0	R	0	APP_SIZE	Aperture size is 0 = 4 kB.

MSP 1 Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.33)

MSP 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Data Queue *N* (*N* = 0 to 47) Head Pointer Registers				
Offset 0x11 8000—80BC			*DQHDPTR*	
31:30	R/W	NI	DQL2NUM [1:0]	Defines which DVP-L2 Interface the data for this queue must be routed though. 0x0 = Route data to DVP-L2 IF #0. 0x1 = Route data to DVP-L2 IF #1. 0x2 = Route data to DVP-L2 IF #2. 0x3 = Reserved

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MSP 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
29:26	R/W	NI	DQSIZE [3:0]	Defines the Data Queue size: 0x0 = 320k bytes 0x1 = 64 bytes 0x2 = 128 bytes 0x3 = 256 bytes 0x4 = 512 bytes 0x5 = 1K bytes 0x6 = 2K bytes 0x7 = 4K bytes 0x8 = 8K bytes 0x9 = 16K bytes 0xA = 32K bytes 0xB = 64K bytes 0xC = 128K bytes 0xD = 256K bytes 0xE = 512K bytes 0xF = 1M bytes
25:0	R/W	NI	DQHP [25:0]	This field defines the lower 26 bits of the 32-bit data queue head pointer. It is updated only when a NEWQ command is received.
Offset 0x11 80C0			*DQLIMIT0*	
31:24	R	0	Reserved	
23:21	R/W	0	DQLIMIT[143:141]	Controls the data queue limit interrupt for queue #47. Once the limit is reached, the interrupt will occur. If DQENLOCK of Data Queue Control Register is enabled, the remaining data for the queue will be discarded until the limit is changed (or disabled). Data queue limit interrupt is disabled. Data queue limit interrupt is at 1/4 queue. Data queue limit interrupt is at 2/4 queue. Data queue limit interrupt is at 3/4 queue. Data queue limit interrupt is at 4/4 queue. Reserved. Reserved. Writing this value has no effect on this field, and this field will remain unchanged.
20:18	R/W	0	DQLIMIT[140:138]	Same as above for data queue #46
17:15	R/W	0	DQLIMIT[137:135]	Same as above for data queue #45
14:12	R/W	0	DQLIMIT[134:132]	Same as above for data queue #44
11:9	R/W	0	DQLIMIT[131:129]	Same as above for data queue #43
8:6	R/W	0	DQLIMIT[128:126]	Same as above for data queue #42
5:3	R/W	0	DQLIMIT[125:123]	Same as above for data queue #41
2:0	R/W	0	DQLIMIT[122:120]	Same as above for data queue #40
Offset 0x11 80C4			*DQLIMIT1*	
31:30	R	0	Reserved	

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MSP 1 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
29:27	R/W	0	DQLIMIT[119:117]	Controls the data queue limit interrupt for queue #39. Once the limit is reached, the interrupt will occur. If DQENLOCK of Data Queue Control Register is enabled, the remaining data for the queue will be discarded until the limit is changed (or disabled). Data queue limit interrupt is disabled. Data queue limit interrupt is at 1/4 queue. Data queue limit interrupt is at 2/4 queue. Data queue limit interrupt is at 3/4 queue. Data queue limit interrupt is at 4/4 queue. Reserved. Reserved. Writing this value has no effect on this field, and this field will remain unchanged.
26:24	R/W	0	DQLIMIT[116:114]	Same as above for data queue #38
23:21	R/W	0	DQLIMIT[113:111]	Same as above for data queue #37
20:18	R/W	0	DQLIMIT[110:108]	Same as above for data queue #36
17:15	R/W	0	DQLIMIT[107:105]	Same as above for data queue #35
14:12	R/W	0	DQLIMIT[104:102]	Same as above for data queue #34
11:9	R/W	0	DQLIMIT[101:99]	Same as above for data queue #33
8:6	R/W	0	DQLIMIT[98:96]	Same as above for data queue #32
5:3	R/W	0	DQLIMIT[95:93]	Same as above for data queue #31
2:0	R/W	0	DQLIMIT[92:90]	Same as above for data queue #30
Offset 0x11 80C8			*DQLIMIT2*	
31:30	R	0	Reserved	
29:27	R/W	0	DQLIMIT[89:87]	Controls the data queue limit interrupt for queue #29. Once the limit is reached, the interrupt will occur. If DQENLOCK of Data Queue Control Register is enabled, the remaining data for the queue will be discarded until the limit is changed (or disabled). Data queue limit interrupt is disabled. Data queue limit interrupt is at 1/4 queue. Data queue limit interrupt is at 2/4 queue. Data queue limit interrupt is at 3/4 queue. Data queue limit interrupt is at 4/4 queue. Reserved. Reserved. Writing this value has no effect on this field, and this field will remain unchanged.
26:24	R/W	0	DQLIMIT[86:84]	Same as above for data queue #28
23:21	R/W	0	DQLIMIT[83:81]	Same as above for data queue #27
20:18	R/W	0	DQLIMIT[80:78]	Same as above for data queue #26
17:15	R/W	0	DQLIMIT[77:75]	Same as above for data queue #25
14:12	R/W	0	DQLIMIT[74:72]	Same as above for data queue #24
11:9	R/W	0	DQLIMIT[71:69]	Same as above for data queue #23
8:6	R/W	0	DQLIMIT[68:66]	Same as above for data queue #22
5:3	R/W	0	DQLIMIT[65:63]	Same as above for data queue #21
2:0	R/W	0	DQLIMIT[62:60]	Same as above for data queue #20
Offset 0x11 80CC			*DQLIMIT3*	

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MSP 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
31:30	R	0	Reserved	
29:27	R/W	0	DQLIMIT[59:57]	Controls the data queue limit interrupt for queue #19. Once the limit is reached, the interrupt will occur. If DQENLOCK of Data Queue Control Register is enabled, the remaining data for the queue will be discarded until the limit is changed (or disabled). Data queue limit interrupt is disabled. Data queue limit interrupt is at 1/4 queue. Data queue limit interrupt is at 2/4 queue. Data queue limit interrupt is at 3/4 queue. Data queue limit interrupt is at 4/4 queue. Reserved. Reserved. Writing this value has no effect on this field, and this field will remain unchanged.
26:24	R/W	0	DQLIMIT[56:54]	Same as above for data queue #18
23:21	R/W	0	DQLIMIT[53:51]	Same as above for data queue #17
20:18	R/W	0	DQLIMIT[50:48]	Same as above for data queue #16
17:15	R/W	0	DQLIMIT[47:45]	Same as above for data queue #15
14:12	R/W	0	DQLIMIT[44:42]	Same as above for data queue #14
11:9	R/W	0	DQLIMIT[41:39]	Same as above for data queue #13
8:6	R/W	0	DQLIMIT[38:36]	Same as above for data queue #12
5:3	R/W	0	DQLIMIT[35:33]	Same as above for data queue #11
2:0	R/W	0	DQLIMIT[32:30]	Same as above for data queue #10
Offset 0x11 80EC			*DQLIMIT4*	
31:30	R	0	Reserved	
29:27	R/W	0	DQLIMIT[29:27]	Controls the data queue limit interrupt for queue #9. Once the limit is reached, the interrupt will occur. If DQENLOCK of Data Queue Control Register is enabled, the remaining data for the queue will be discarded until the limit is changed (or disabled). Data queue limit interrupt is disabled. Data queue limit interrupt is at 1/4 queue. Data queue limit interrupt is at 2/4 queue. Data queue limit interrupt is at 3/4 queue. Data queue limit interrupt is at 4/4 queue. Reserved. Reserved. Writing this value has no effect on this field, and this field will remain unchanged.
26:24	R/W	0	DQLIMIT[26:24]	Same as above for data queue #8
23:21	R/W	0	DQLIMIT[23:21]	Same as above for data queue #7
20:18	R/W	0	DQLIMIT[20:18]	Same as above for data queue #6
17:15	R/W	0	DQLIMIT[17:15]	Same as above for data queue #5
14:12	R/W	0	DQLIMIT[14:12]	Same as above for data queue #4
11:9	R/W	0	DQLIMIT[11:9]	Same as above for data queue #3
8:6	R/W	0	DQLIMIT[8:6]	Same as above for data queue #2
5:3	R/W	0	DQLIMIT[5:3]	Same as above for data queue #1
2:0	R/W	0	DQLIMIT[2:9]	Same as above for data queue #0

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MSP 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x11 80D0			*DQHDPTRBASE*	
31:26	R/W	0	DQHP	This is the upper 6 bits of the 32-bit data queue head pointer, and is the same for all 64 queues.
25:0			Reserved	
Data Queue Interrupt Mask Registers				
Offset 0x11 80D4			*DQI0MSKHI*	
31:16			Reserved	
15:0	R/W	0	DQI0MSK [47:32]	0 = Corresponding data queue interrupt is masked. 1 = Corresponding data queue interrupt is enabled and routed to MQMINT[0].
Offset 0x11 80D8			*DQI0MSKLO*	
31:0	R/W	0	DQI0MSK [31:0]	0 = Corresponding data queue interrupt is disabled. 1 = Corresponding data queue interrupt is enabled and routed to MQMINT[0].
Offset 0x11 80DC			*DQI1MSKHI*	
31:16			Reserved	
15:0	R/W	0	DQI1MSK [47:32]	0 = Corresponding data queue interrupt is masked. 1 = Corresponding data queue interrupt is enabled and routed to MQMINT[1].
Offset 0x11 80E0			*DQI1MSKLO*	
31:0	R/W	0	DQI1MSK [31:0]	0 = Corresponding data queue interrupt is disabled. 1 = Corresponding data queue interrupt is enabled and routed to MQMINT[1].
Data Queue Interrupt Status Registers				
Offset 0x11 80E4			*DQISTATHI*	
31:16		-	Unused	
15:0	 R W	0	DQISTAT [47:32]	These bits reflect the interrupt pending status of the queues. The MQM will set the corresponding bit in this register regardless of whether the corresponding bit in the DQIMSK registers was masked or not. 0 = Corresponding data queue interrupt has not occurred. 1 = Corresponding data queue interrupt is pending. 0 = No effect 1 = Corresponding data queue interrupt is reset by the host.
Offset 0x11 80E8			*DQISTATLO*	
31:0	 R W	0	DQISTAT [31:0]	These bits reflect the interrupt pending status of the queues. The MQM will set the corresponding bit in this register regardless of whether the corresponding bit in the DAIMSK register was masked or not. 0 = Corresponding data queue interrupt has not occurred. 1 = Corresponding data queue interrupt is pending. 0 = No effect 1 = Corresponding data queue interrupt is reset by the host.
Data Queue Interrupt Threshold Registers				
Offset 0x11 80F0			*DQTHRESH0*	

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MSP 1 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
31:30	R/W	0	DQITHRESH [95:94]	Controls the Data Queue Threshold Interrupt for Queue #47. 0x0 = Data Queue Threshold Interrupt is disabled. 0x1 = DQ Threshold Interrupt is at 1/4 queue. 0x2 = DQ Threshold Interrupt is at 1/2 queue. 0x3 = Writing this value has no effect on this field, and this field will remain unchanged.
29:28	R/W	0	DQITHRESH[93:92]	Same as above for Queue #46.
27:26	R/W	0	DQITHRESH[91:90]	Same as above for Queue #45.
25:24	R/W	0	DQITHRESH[89:88]	Same as above for Queue #44.
23:22	R/W	0	DQITHRESH[87:86]	Same as above for Queue #43.
21:20	R/W	0	DQITHRESH[85:84]	Same as above for Queue #42.
19:18	R/W	0	DQITHRESH[83:82]	Same as above for Queue #41.
17:16	R/W	0	DQITHRESH[81:80]	Same as above for Queue #40.
15:14	R/W	0	DQITHRESH[79:78]	Same as above for Queue #39.
13:12	R/W	0	DQITHRESH[77:76]	Same as above for Queue #38.
11:10	R/W	0	DQITHRESH[75:74]	Same as above for Queue #37.
9:8	R/W	0	DQITHRESH[73:72]	Same as above for Queue #36.
7:6	R/W	0	DQITHRESH[71:70]	Same as above for Queue #35.
5:4	R/W	0	DQITHRESH[69:68]	Same as above for Queue #34.
3:2	R/W	0	DQITHRESH[67:66]	Same as above for Queue #33.
1:0	R/W	0	DQITHRESH[65:64]	Same as above for Queue #32.
Offset 0x11 80F4			*DQTHRESH1*	
31:30	R/W	0	DQITHRESH [63:62]	Controls the Data Queue Threshold Interrupt for Queue #31. 0x0 = Data Queue Threshold Interrupt is disabled. 0x1 = DQ Threshold Interrupt is at 1/4 queue. 0x2 = DQ Threshold Interrupt is at 1/2 queue. 0x3 = Writing this value has no effect on this field, and this field will remain unchanged.
29:28	R/W	0	DQITHRESH [61:60]	Same as above for Queue #30.
27:26	R/W	0	DQITHRESH [59:58]	Same as above for Queue #29.
25:24	R/W	0	DQITHRESH [57:56]	Same as above for Queue #28.
23:22	R/W	0	DQITHRESH [55:54]	Same as above for Queue #27.
21:20	R/W	0	DQITHRESH [53:52]	Same as above for Queue #26.
19:18	R/W	0	DQITHRESH [51:50]	Same as above for Queue #25.
17:16	R/W	0	DQITHRESH [49:48]	Same as above for Queue #24.
15:14	R/W	0	DQITHRESH [47:46]	Same as above for Queue #23.
13:12	R/W	0	DQITHRESH [45:44]	Same as above for Queue #22.
11:10	R/W	0	DQITHRESH [43:42]	Same as above for Queue #21.
9:8	R/W	0	DQITHRESH [41:40]	Same as above for Queue #20.
7:6	R/W	0	DQITHRESH [39:38]	Same as above for Queue #19.
5:4	R/W	0	DQITHRESH [37:36]	Same as above for Queue #18.
3:2	R/W	0	DQITHRESH [35:34]	Same as above for Queue #17.

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MSP 1 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
1:0	R/W	0	DQITHRESH [33:32]	Same as above for Queue #16.
Offset 0x11 80F8			*DQTHRESH2*	
31:30	R/W	0	DQITHRESH [31:0]	Controls the Data Queue Threshold Interrupt for Queue #15. 0x0 = Data Queue Threshold Interrupt is disabled. 0x1 = DQ Threshold Interrupt is at 1/4 queue. 0x2 = DQ Threshold Interrupt is at 1/2 queue. 0x3 = Writing this value has no effect on this field, and this field will remain unchanged.
29:28	R/W	0	DQITHRESH [29:28]	Same as above for Queue #14.
27:26	R/W	0	DQITHRESH [27:26]	Same as above for Queue #13.
25:24	R/W	0	DQITHRESH [25:24]	Same as above for Queue #12.
23:22	R/W	0	DQITHRESH [23:22]	Same as above for Queue #11.
21:20	R/W	0	DQITHRESH [21:20]	Same as above for Queue #10.
19:18	R/W	0	DQITHRESH [19:18]	Same as above for Queue #9.
17:16	R/W	0	DQITHRESH [17:16]	Same as above for Queue #8.
15:14	R/W	0	DQITHRESH [15:14]	Same as above for Queue #7.
13:12	R/W	0	DQITHRESH [13:12]	Same as above for Queue #6.
11:10	R/W	0	DQITHRESH [11:10]	Same as above for Queue #5.
9:8	R/W	0	DQITHRESH [9:8]	Same as above for Queue #4.
7:6	R/W	0	DQITHRESH [7:6]	Same as above for Queue #3.
5:4	R/W	0	DQITHRESH [5:4]	Same as above for Queue #2.
3:2	R/W	0	DQITHRESH [3:2]	Same as above for Queue #1.
1:0	R/W	0	DQITHRESH [1:0]	Same as above for Queue #0.
Data Queue Control Registers				
Offset 0x11 80FC			*DQCTL*	
31:4		-	Reserved	
3	R/W	0	DQENLOCK	0 = Disable queue lock mechanism for Limit Interrupt. 1 = Enable the queue lock mechanism for limit interrupt to prevent data queues from overrunning. If the data queue reaches the limit, the following data for the corresponding queue will be discarded until the limit value is changed or the limit interrupt is disabled.
2:1	R/W	0	DQRUN_STOP	11 = Reserved 10 = RUN - Enable MQM to process data. 01 = STOP - The MQM will stop at the next NEWQ command. 00 = NO CHANGE - No change from the last status (If the MQM was running, it will continue to run. If the MQM was stopped, it will not start).
0	R/W	0	DQRST	0 = No effect 1 = Software reset. Resets the whole MQM and the MQM FIFO but does not reset the MQM register values. This bit will auto-clear after the MQM reset procedure is complete.
GP/HS Registers				
Offset 0x11 8100			*GPHSCTL*	
31:16		-	Unused	

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MSP 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
15	R/W	0	AVSYNC_FN	GP/HS Interface mode decides the function of AVSYNC output. 0 = The AVSYNC output creates a pulse on the first valid byte of the packet. This is intended to interface with Philips Link Devices. 1 = The AVSYNC output creates a "blank" or a PACKETGAP when no packets are output.
14	R/W	0	CC_LOCK_AB	Packet Insertion Continuity Count Control 0 = Packets A and B have their own continuity counters. 1 = Packets A and B both increment their continuity counters on any packet insertion.
13	R/W	0	CC_UPD_EN	Packet Insertion Continuity Counter Enable 0 = Continuity counter insertion disabled. 1 = Continuity counter insertion enabled. When this field is written with a '1', the CC_INIT_VAL register field will also be updated with the host write data.
12	R/W	0	INS_MODE	Packet insertion mode 0 = Automatic packet insertion mode 1 = Manual packet insertion mode
11	R/W	0	INS_PKTB	0 = Packet B insert disabled 1 = Packet B insert enabled
10	R/W	0	INS_PKTA	0 = Packet A insert disabled 1 = Packet A insert enabled
9	R/W	0	INS_EN	0 = Packet insertion disabled 1 = Packet insertion enabled
8	R/W	0	INPUTSEL	0 = GP/HS uses de-scrambled input. 1 = GP/HS uses scrambled Input.
7:6	R/W	0x3	GPIF_MODE [1:0]	Defines the GP/HS interface mode 00 = GP interface mode 01 = HS Data interface mode 10 = IEEE 1394 interface mode 11 = Disabled
5:2	R/W	0	CC_INIT_VAL [3:0]	Defines the Initial value of the packet insertion Continuity counters. This value will only be loaded into the registers when the CC_UPD_EN bit is written with a '1'. If the CC_UPD_EN bit is written with a '0', this field will not change. This is to prevent accidental change of this field.
1			Reserved	
0	R/W	1	GP_DIR	0 = GP Interface is in the output mode. 1 = GP Interface is in the input mode.
Offset 0x11 8104			*PKTSIZE*	
31:16		-	Unused	
15:10			Reserved	
9	R/W	0	DVB_DSS	This field is only used by the packet insertion logic to insert the Continuity count into inserted packets at the correct place. 0 = GP/HS Output interface is in DSS mode. 1 = GP/HS Output interface is in DVB mode.
8	R/W	0	DSS_PKTSIZE	This field is only used by the packet insertion logic to insert the Continuity count into the inserted packets at the correct place. 0 = DSS output packet is 130 bytes. 1 = DSS output packet is 140 bytes, of which the first 10 bytes comprise an additional header.

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MSP 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
7:0	R/W	0xBC	PKTSIZE	Defines the packet size. Use 188 for DVB, 130 for DSS, and 140 for DSS with IEEE1394 padding.
Offset 0x11 8108			*INSTHRESH*	
31:16		-	Unused	
15:0	R/W	0	INS_THRESH	Defines the packet insertion threshold. If enabled, the packet insertion logic will insert packets into the GP/HS output interface after the number of packets specified in this field.
Offset 0x11 8110			*INSSTAT*	
31:2		-	Unused	
1	R	0	INSB_STATUS	Reports the insertion status for PKT-B. 0 = Packet B not being inserted. 1 = Packet B will be inserted next.
0	R	0	INSA_STATUS	Reports the insertion status for PKT-A. 0 = Packet A not being inserted. 1 = Packet A will be inserted next.
Offset 0x11 8114			*INSCOUNT*	
31:16		-	Unused	
15:0	R/W	0	INS_COUNT	Returns the current value of the packet insertion counter.
Offset 0x11 8118			*PKTADDR*	
31:9		-	Unused	
8:0	W	0	PKTADDR	Returns 0. PacketRAM address where data has to be written. Two bytes must be written into the PacketRAM at the same time. Addresses for packet A - 188 to 281 Addresses for packet B - 282 to 375
Offset 0x11 811C			*PKTDATA*	
31:16		-	Unused	
15:0	W	0	PKTDATA	Returns 0. Data to be written into the PacketRAM. Writing to this register also writes data into the RAM. The PKTADDR register must be written to first with the PacketRAM address before data is written in this register. PKTDATA[7:0] = lower addressed byte. PKTDATA[15:8] = higher addressed byte.
Packet Framer Registers				
Offset 0x11 8200			*FRMRCTL*	
31:16		-	Unused	
15	R/W	1	DVB_DSS	0 = The Framer is in DSS mode. 1 = The Framer is in DVB mode.
14	R/W	0	SYNDET	0 = Normal Sync detection 1 = Forces the Packet Framer into sync detection at the end of the current transport packet, even if the framer is in sync. The Packet Framer will clear this bit automatically on sync detection.
13	R/W	0	TEI_EN	Defines the behavior of the Packet Framer on Transport Error Indicator (TEI) detection for DVB packets only. No effect for DSS packets. 0 = If the TEI bit is '1', the entire transport packet is discarded and is not passed on to the RISC or used for PCR recovery 1 = Ignores the TEI bit in the TP header.

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MSP 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
12	R/W	0	DSS140_IN	Defines the input DSS packet size. 0 = Input DSS packet size is 130 bytes. 1 = Input DSS packet size is 140 bytes. This is a playback from the IEEE 1394 interface. The first 10 bytes is the IEEE 1394 header followed by a 130-byte DSS packet.
11	R/W	0	DSS140_OUT	Defines the output DSS packet size. This bit is only effective when the DSS140_IN bit is a '1'. 0 = DSS output packets are 130 bytes. 1 = DSS output packets are 140 bytes. The first 10 bytes are a IEEE 1394 header followed by a 130-byte DSS Packet.
10	R/W	0	CHSYNC_DLY	Delays the CHSYNC input signal for 140-byte input DSS Packets by 10 clocks. This is only effective when the DSS140_IN bit is a '1'. 0 = No delay for SYNC. No PID matching is possible in the Packet Framer. 1 = SYNC is delayed by 10 clocks to line up with the first valid 130-byte DSS packet so that the Framer can do a PID Matching on a 140-byte input DSS Packet.
9	R/W	0	CHORD	Defines the bit order in the CHDATA[7:0] input. 0 = Sets bit 7 to be msb. 1 = Sets bit 0 to be msb.
8	R/W	0	CHERR_EN	0 = Ignores CHERR input signal. 1 = Reserved
7:0	R/W	47	SYNCBP	Defines the Sync byte pattern for DVB. The default is 47h. This field is not used for DSS.
Offset 0x11 8204			*FRMRSYNC*	
31:16		-	Unused	
15	R/W	0	FRAMEEN	0 = Disables Packet Framer. No data is passed to the RISC Engine. 1 = Enables Packet Framer. Data is passed to the RISC Engine.
14	R/W	0	CHCLK_SYNC	0 = The CHCLK input signal is asynchronous to MSP Clock. The max frequency of the CHCLK signal cannot be more than 27 MHz. 1 = CHCLK is same frequency and is synchronous to MSP Clock.
13	R/W	0	SYNCSEL	DSS Synchronization Select 0 = Synchronizes with the Sync bit in the packet. 1 = Synchronizes with the CHSYNC input signal.
12	R/W		BYPASSEN	0 = Normal packet framing. All input data received in the channel interface is passed on to the RISC Engine after framing and synchronizing. 1 = Bypass. All input data is passed on to the RISC Engine without any framing or synchronizing.
11	R/W	-	BYTE_ALIGN	Force byte alignment - used for testing purposes. 0 = Normal operation - allows the Packet Framer to sync on any bit alignment. 1 = Byte alignment - forces the Packet Framer to align to the bytes that are presented on the parallel data input and search for the sync byte.
10		0	Reserved	
9:5	R/W	1	SYNCDRP	SYNC DROP - The number of consecutive Sync bytes (DVB) or bits (DSS) that must be lost to constitute a sync drop. (Sync bytes/bits are spaced one TP apart). A value of "0" is invalid.

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MSP 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
4:0	R/W	1	SYNCLCK	SYNC LOCK - This field contains the number of consecutive sync bytes that must be detected before sync is locked. (Sync bytes/bits are spaced one TP apart). This value must be between 1 and 31. A value of '0' disables Sync Locking.
Offset 0x11 8208			*PIDMASK*	
31:16		-	Unused	
15:0	R/W	1FFF	PIDMASK	This field defines the 16-bit PID Masking pattern used by the PID Filter. A '1' in a bit field allows that bit to be compared, and a '0' masks that bit out. For DVB, use a value of 0x1FFF. For DSS, use a value of 0x0FFF. All other values must only be used for diagnostic purposes.
Offset 0x11 820C			*PIDCTL*	
31:13		-	Unused	
12:5	R/W	0	Reserved	
4	R/W	0	TSEN	0 = Disables Timestamp insertion. 1 = Enables Timestamp Insertion. If enabled, 4 extra bytes (32-bit timestamp) are inserted into the stream.
3	R/W	0	PIDEN	0 = Disables PID filtering. If PID filtering is disabled, the entire packet is sent to the RISC Engine. 1 = Enables PID filtering. If enabled, two extra bytes denoting the PID match number are sent to the RISC engine with the entire packet.
2	R/W	0	NMTCHEN	0 = Drop packets are not matched by the PID filter. 1 = Send packets are not matched by the PID filter downstream for processing.
1	R/W	0	NUMPIDS	0 = Number of PIDs = 40 1 = Number of PIDs = 64
0	R/W	0	RSTPEAK	Ignore read value. 0 = No effect 1 = Resets FIFO Peak Detector in the PEAKVAL register.
Offset 0x11 8210			*PEAKVAL*	
31:8		-	Unused	
7:0	R	0	PEAKVAL	This field contains the maximum value of data in the FIFO. It is only intended to be used for debugging.
Offset 0x11 8214—8258			*Reserved*	
DSS Bit Rate Registers				
Offset 0x11 825C			*DSS_BITRATE*	
31:16		-	Unused	
15:0	R/W	0	DSSBITRATE	DSS Bit Rate [15:0] The value set by the host in this register is used by the Packet Framer as part of the 10-byte DSS packet header. Specifically, DSSBITRATE[15:8] is byte 4 and DSSBITRATE[7:0] is byte 5.

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MSP 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x11 8300—83FC			*PIDTABLE*	
31:16		-	Unused	
15	R/W	NI	PIDVALID	0 = PID entry is Invalid. 1 = PID entry is Valid.
14	R/W	NI	PCRPKT	0 = PID does not contain PCR. 1 = PID contains PCR. A PCR will be extracted from a packet with this PID (if a PCR is present in it).
13	R/W	NI	1394EN	0 = Do not route this packet to the GP/HS interface. 1 = This packet can be sent to the GP/HS interface.
12:0	R/W	NI	PID	13-bit PID value

MSP 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
RISC Engine Registers				
Offset 0x11 8400			*RISCDBG0*	
31:16		-	Unused	
15:8	R		RISC_R0	Returns the value of register r0.
7:0	R		RISC_R1	Returns the value of register r1.
Offset 0x11 8404			*RISCDBG1*	
31:16		-	Unused	
15:8	R		RISC_R2	Returns the value of register r2.
7:0	R		RISC_R3	Returns the value of register r3.
Offset 0x11 8408			*RISCDBG2*	
31:16		-	Unused	
15:8	R		RISC_R4	Returns the value of register r4.
7:0	R		RISC_R5	Returns the value of register r5.
Offset 0x11 840C			*RISCDBG3*	
31:16		-	Unused	
15:8	R	NI	RISC_R6	Returns the value of register r6.
7:0	R	NI	RISC_R7	Returns the value of register r7.
Offset 0x11 8410			*RISCDBG4*	
31:16		-	Unused	
15:8	R	NI	RISC_RC1	Returns the value of register rc1.
7:0	R	NI	RISC_RC2	Returns the value of register rc2.
Offset 0x11 8414			*RISCDBG5*	
31:16		-	Unused	
15:8	R	NI	RISC_LOOPC	Returns the value of register loopc.

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MSP 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
7:0	R	NI	RISC_TCCNT	Returns the value of register tccnt.
Offset 0x11 8418			*RISCDBG6*	
31:16		-	Unused	
15:8	R	NI	RISC_DSCRM	Returns the value of register de-scram.
7:0	R	NI	RISC_RP	Returns the value of register rp.
Offset 0x11 841C			*RISCDBG7*	
31:16		-	Unused	
15:0	R	NI	RISCCPUCTL	Returns the value of register cpuctl.
Offset 0x11 8420			*RISCDBG8*	
31:16		-	Unused	
9:0	R	NI	RISC_PC	Returns the value of register pc.
Offset 0x11 8424			*RISCDBG9*	
31:10		-	Unused	
9:0	R	NI	RISC_BTA	Returns the value of register bta.
Offset 0x11 8428			*RISCDBG10*	
31:10		-	Unused	
9:0	R	NI	RISC_BBTA	Returns the value of register bbta.
Offset 0x11 842C			*RISCDBG11*	
31:8		-	Unused	
7:0	R	NI	RISC_FLAGS	Returns the value of risc flags. Bit 7 = ZERO Bit 6 = ZERO Bit 5 = GT Bit 4 = GT Bit 3 = LT Bit 2 = LT Bit 1 = OVR Bit 0 = LOOPC_ZERO
Offset 0x11 8430			*RISCCTL*	
31:2		-	Unused	
1	R/W	1	RISC_STOP	0 = RISC is running. 1 = RISC is stopped.
0	W	0	RISC_SSTEP	Always returns 0. 0 = No Effect 1 = Forces RISC Engine to execute one instruction.
Offset 0x11 8434			*HSFCTL*	
31:2		-	Unused	
1:0	R/W	0	SEC_MODE	Defines the Section Filtering Type. 00 = 8-byte Section Filter Type 01 = 12-byte Section Filter Type 10 = 8-byte Section Range Filter Type 11 = Reserved

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MSP 1 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
De-Scrambler Keys				
*Offset 0x11 8600 + n*8*			*KEYnEVN0 (n = 0 to F)*	
31:0	R/W	NI	KEY_EVN [31:0]	De-Scrambler Even Key. At power up, the de-scrambler key table is invalid and must be initialized by software.
*Offset 0x11 8604 + n*8*			*KEYnEVN1 (n = 0 to F)*	
31:0	R/W	NI	KEY_EVN [63:32]	De-Scrambler Even Key. At power up, the de-scrambler key table is invalid and must be initialized by software.
*Offset 0x11 8680 + n*8*			*KEYnODD0 (n = 0 to F)*	
31:0	R/W	NI	KEY_ODD [31:0]	De-Scrambler Odd Key. At power up, the de-scrambler key table is invalid and must be initialized by software.
*Offset 0x11 8684 + n*8*			*KEYnODD1 (n = 0 to F)*	
31:0	R/W	NI	KEY_ODD [63:32]	De-Scrambler Odd Key. At power up, the de-scrambler key table is invalid and must be initialized by software.
Multi-2 and Copy Protect Keys				
Offset 0x11 8700			*M2SYSKEY0*	
31:0	R/W	0	SYS_KEY [31:0]	Multi-2 System Key
Offset 0x11 8704			*M2SYSKEY1*	
31:0	R/W	0	SYS_KEY [63:32]	Multi-2 System Key
Offset 0x11 8708			*M2SYSKEY2*	
31:0	R/W	0	SYS_KEY [95:64]	Multi-2 System Key
Offset 0x11 870C			*M2SYSKEY3*	
31:0	R/W	0	SYS_KEY [127:96]	Multi-2 System Key
Offset 0x11 8710			*M2SYSKEY4*	
31:0	R/W	0	SYS_KEY [159:128]	Multi-2 System Key
Offset 0x11 8714			*M2SYSKEY5*	
31:0	R/W	0	SYS_KEY [191:160]	Multi-2 System Key
Offset 0x11 8718			*M2SYSKEY6*	
31:0	R/W	0	SYS_KEY [223:192]	Multi-2 System Key
Offset 0x11 871C			*M2SYSKEY7*	
31:0	R/W	0	SYS_KEY [255:224]	Multi-2 System Key
Offset 0x11 8720			*CPKEYEVEN0*	
31:0	R/W	0	CP_KEY_EVN [31:0]	Copy Protection Even Key
Offset 0x11 8724			*CPKEYEVEN1*	
31:0	R/W	0	CP_KEY_EVN [63:32]	Copy Protection Even Key
Offset 0x11 8728			*CPKEYODD0*	
31:0	R/W	0	CP_KEY_ODD [31:0]	Copy Protection Odd Key
Offset 0x11 872C			*CPKEYODD1*	
31:0	R/W	0	CP_KEY_ODD [63:32]	Copy Protection Odd Key
De-Scrambler/Copy Protect Initialization Vectors				

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MSP 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x11 8730			*DSCIVCBC0*	
31:0	R/W	0	DSC_IV_CBC [31:0]	De-scrambler IV CBC
Offset 0x11 8734			*DSCIVCBC1*	
31:0	R/W	0	DSC_IV_CBC [63:32]	De-scrambler IV CBC
Offset 0x11 8738			*DSCIVOFB0*	
31:0	R/W	0	DSC_IV_OFB [31:0]	De-scrambler IV OFB
Offset 0x11 873C			*DSCIVOFB1*	
31:0	R/W	0	DSC_IV_OFB [63:32]	De-scrambler IV OFB
Offset 0x11 8740			*CPIVCBC0*	
31:0	R/W	0	CP_IV_CBC [31:0]	Copy Protect IV CBC
Offset 0x11 8744			*CPIVCBC1*	
31:0	R/W	0	CP_IV_CBC [63:32]	Copy Protect IV CBC
Offset 0x11 8748			*CPIVOFB0*	
31:0	R/W	0	CP_IV_OFB [31:0]	Copy Protect IV OFB
Offset 0x11 874C			*CPIVOFB1*	
31:0	R/W	0	CPIV_OFB [63:32]	Copy Protect IV OFB
De-Scrambler Modes				
Offset 0x11 8750			*MODEPAD*	
31:21		-	Unused	
20:16	R/W	0	CP_MODE [4:0]	Copy Protect Mode Full Block / Residual Block / Solitary Block 0x0 = None / None / None 0x1 = DES-ECB / None / None 0x2 = DES-ECB / DES-OFB(PB) / None 0x3 = DES-ECB / DES-OFB(PB) / DES-OFB(IV) 0x4 = DES-ECB / DES-OFB(IV) / None 0x5 = DES-ECB / DES-OFB(IV) / DES-OFB(IV) 0x6 = Reserved / Reserved / Reserved 0x7 = DES-CBC / None / None 0x8 = DES-CBC / DES-OFB(PB) / None 0x9 = DES-CBC / DES-OFB(PB) / DES-OFB(IV) 0xa = DES-CBC / DES-OFB(IV) / None 0xb = DES-CBC / DES-OFB(IV) / DES-OFB(IV) 0xc—0xf = Reserved / Reserved / Reserved
15:13		-	Unused	

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MSP 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
12:8	R/W	0	DSC_MODE [4:0]	De-Scrambler Mode Full Block / Residual Block / Solitary Block 0x00 = None / None / None 0x01 = DES-ECB / None / None 0x02 = DES-ECB / DES-OFB(PB) / None 0x03 = DES-ECB / DES-OFB(PB) / DES-OFB(IV) 0x04 = DES-ECB / DES-OFB(IV) / None 0x05 = DES-ECB / DES-OFB(IV) / DES-OFB(IV) 0x06 = Reserved / Reserved / Reserved 0x07 = DES-CBC / None / None 0x08 = DES-CBC / DES-OFB(PB) / None 0x09 = DES-CBC / DES-OFB(PB) / DES-OFB(IV) 0x0a = DES-CBC / DES-OFB(IV) / None 0x0b = DES-CBC / DES-OFB(IV) / DES-OFB(IV) 0x0c = Reserved / Reserved / Reserved 0x0d = DVB / DVB / DVB 0x0e = MULTI2 / MULTI2 / MULTI2 0x0f—0x10 = Reserved / Reserved / Reserved 0x11 = 3DES-ECB / None / None 0x12 = 3DES-ECB / 3DES-OFB(PB) / None 0x13 = 3DES-ECB / 3DES-OFB(PB) / 3DES-OFB(IV) 0x14 = 3DES-ECB / 3DES-OFB(IV) / None 0x15 = 3DES-ECB / 3DES-OFB(IV) / 3DES-OFB(IV) 0x16 = Reserved / Reserved / Reserved 0x17 = 3DES-CBC / None / None 0x18 = 3DES-CBC / 3DES-OFB(PB) / None 0x19 = 3DES-CBC / 3DES-OFB(PB) / 3DES-OFB(IV) 0x1a = 3DES-CBC / 3DES-OFB(IV) / None 0x1b = 3DES-CBC / 3DES-OFB(IV) / 3DES-OFB(IV) 0x1c—0x1f = Reserved / Reserved / Reserved
7:0	R/W	0	PAD_CHAR	Pad Character
Offset 0x11 8754			*Reserved*	
Offset 0x11 8758			*Reserved*	

MSP 1 REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
PI-Bus Configuration Registers				
Offset 0x11 8C00			*MSPRST*	
31:5		-	Unused	
4	W	NI	RST_GPHS	Ignore read value. 0 = No Effect 1 = Writing a ’1’ will automatically reset the GP/HS. This bit will auto-clear.
3	W	NI	RST_MQM	Ignore read value 0 = No Effect 1 = Writing a ’1’ will automatically reset the MQM. This bit will auto-clear.

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MSP 1 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
2	W	NI	RST_DESC	Ignore read value 0 = No Effect 1 = Writing a '1' will automatically reset the de-scrambler. This bit will auto-clear.
1	W	NI	RST_RISC	Ignore read value 0 = No Effect 1 = Writing a '1' will automatically reset the RISC Engine. This bit will auto-clear.
0	W	NI	RST_FRMR	Ignore read value 0 = No Effect 1 = Writing a '1' will automatically reset the Packet Framer and the PCR logic. This bit will auto-clear.

MSP 1 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
MSP Interrupt Registers				
Offset 0x11 8FE0			*STB_MSPINTST*	
31:20		-	Unused	
19:0	R	0	STB_MSPINTST	The MSP Interrupt Status This register allows software to check an interrupt status for pending interrupts. Each bit controls each internal interrupt source. 0 = Corresponding interrupt is not pending. 1 = Corresponding interrupt is pending.
Offset 0x11 8FE4			*STB_MSPINTENA*	
31:20		-	Unused	
19:0	R/W	0	STB_MSPINTENA	The MSP Interrupt Enable This register allows software to selectively enable an interrupt. Each bit controls each internal interrupt source. 0 = Corresponding interrupt is disabled. 1 = Corresponding interrupt is enabled.
Offset 0x11 8FE8			*STB_MSPINTCLR*	
31:20		-	Unused	
19:0	W	NI	STB_MSPINTCLR	The MSP Interrupt Clear This register allows software to reset an interrupt. Each bit controls each internal interrupt source. Ignore read data. 0 = Corresponding interrupt is not cleared. 1 = Corresponding interrupt is cleared.
Offset 0x11 8FEC			*STB_MSPINTSET*	
31:20		-	Unused	
19:0	W	NI	STB_MSPINTSET	The MSP Interrupt Set This register allows software to set an interrupt. Each bit controls each internal interrupt source. Ignore read data. 0 = Corresponding interrupt is not set. 1 = Corresponding interrupt is set.

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MSP 1 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x11 8FF4			*POWERDOWN*	
31	R/W	0	POWER_DOWN	Powerdown register for the module 0 = Normal operation of the peripheral. This is the reset value. 1 = Module is powered down and module clock can be removed. At powerdown, module responds to all reads with DEADABBA (except for reads of powerdown bit) and all writes with ERR ACK (except for writes to powerdown bit).
30:0		-	Unused	Ignore during writes and read as zeroes.
Offset 0x11 8FFC			*MODULEID*	
31:16	R	0x010E	MODULEID [15:0]	Returns "0x010E"
15:12	R	0x2	MAJREV [3:0]	Major Revision of the MSP. 0 = PNX8526 rev A 2 = PNX8526 rev B with ICAM 4 = PNX8526 rev B without ICAM
11:8	R	0	MINREV [3:0]	Minor Revision of the MSP
7:0	R	0x07	APERSIZE [7:0]	0x07 = Returns ”0x07.” The MSP needs an aperture size of 32 kB.

MSP 2 Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.33)

MSP 2 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Data Queue N (N=0 to 47) Head Pointer Registers				
Offset 0x12 0000—00BC			*DQHDPTR*	
Offset 0x12 00D0			*DQHDPTRBASE*	
Data Queue Interrupt Mask Registers				
Offset 0x12 00D4			*DQI0MSKHI*	
Offset 0x12 00D8			*DQI0MSKLO*	
Offset 0x12 00DC			*DQI1MSKHI*	
Offset 0x12 00E0			*DQI1MSKLO*	
Data Queue Interrupt Status Registers				
Offset 0x12 00E4			*DQISTATHI*	
Offset 0x12 00E8			*DQISTATLO*	
Data Queue Interrupt Threshold Registers				
Offset 0x12 00F0			*DQTHRESH0*	
Offset 0x12 00F4			*DQTHRESH1*	
Offset 0x12 00F8			*DQTHRESH2*	
Data Queue Control Registers				
Offset 0x12 00FC			*DQCTL*	
GP/HS Registers				

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MSP 2 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x12 0100			*GPHSCTL*	
Offset 0x12 0104			*PKTSIZE*	
Offset 0x12 0108			*INSTHRESH*	
Offset 0x12 0110			*INSSTAT*	
Offset 0x12 0114			*INSCOUNT*	
Offset 0x12 0118			*PKTADDR*	
Offset 0x12 011C			*PKTDATA*	
Packet Framer Registers				
Offset 0x12 0200			*FRMRCTL*	
Offset 0x12 0204			*FRMRSYNC*	
Offset 0x12 0208			*PIDMASK*	
Offset 0x12 020C			*PIDCTL*	
Offset 0x12 0210			*PEAKVAL*	
Offset 0x12 0214—0258			*Reserved*	
DSS Bit Rate Registers				
Offset 0x12 025C			*DSS_BITRATE*	
Offset 0x12 0300—03FC			*PIDTABLE*	
RISC Engine Registers				
Offset 0x12 0400			*RISCDBG0*	
Offset 0x12 0404			*RISCDBG1*	
Offset 0x12 0408			*RISCDBG2*	
Offset 0x12 040C			*RISCDBG3*	
Offset 0x12 0410			*RISCDBG4*	
Offset 0x12 0414			*RISCDBG5*	
Offset 0x12 0418			*RISCDBG6*	
Offset 0x12 041C			*RISCDBG7*	
Offset 0x12 0420			*RISCDBG8*	
Offset 0x12 0424			*RISCDBG9*	
Offset 0x12 0428			*RISCDBG10*	
Offset 0x12 042C			*RISCDBG11*	
Offset 0x12 0430			*RISCCTL*	
Offset 0x12 0434			*HSFCTL*	
De-Scrambler Keys				
*Offset 0x12 0600 + n*8*			*KEYnEVN0 (n = 0 to F)*	
*Offset 0x12 0604 + n*8*			*KEYnEVN1 (n = 0 to F)*	
*Offset 0x12 0680 + n*8*			*KEYnODD0 (n = 0 to F)*	
*Offset 0x12 0684 + n*8*			*KEYnODD1 (n = 0 to F)*	
Multi-2 Keys				
Offset 0x12 0700			*M2SYSKEY0*	

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MSP 2 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x12 0704			*M2SYSKEY1*	
Offset 0x12 0708			*M2SYSKEY2*	
Offset 0x12 070C			*M2SYSKEY3*	
Offset 0x12 0710			*M2SYSKEY4*	
Offset 0x12 0714			*M2SYSKEY5*	
Offset 0x12 0718			*M2SYSKEY6*	
Offset 0x12 071C			*M2SYSKEY7*	
Copy Protect Keys				
Offset 0x12 0720			*CPKEYEVEN0*	
Offset 0x12 0724			*CPKEYEVEN1*	
Offset 0x12 0728			*CPKEYODD0*	
Offset 0x12 072C			*CPKEYODD1*	
De-Scrambler/Copy Protect Initialization Vectors				
Offset 0x12 0730			*DSCIVCBC0*	
Offset 0x12 0734			*DSCIVCBC1*	
Offset 0x12 0738			*DSCIVOFB0*	
Offset 0x12 073C			*DSCIVOFB1*	
Offset 0x12 0740			*CPIVCBC0*	
Offset 0x12 0744			*CPIVCBC1*	
Offset 0x12 0748			*CPIVOFB0*	
Offset 0x12 074C			*CPIVOFB1*	
De-Scrambler Modes				
Offset 0x12 0750			*MODEPAD*	
Offset 0x12 0754			*Reserved*	
Offset 0x12 0758			*Reserved*	
PI Bus Configuration Registers				
Offset 0x12 0C00			*MSPRST*	
MSP Interrupt Registers				
Offset 0x12 0FE0			*STB_DMAINTST*	
Offset 0x12 0FE4			*STB_DMAINTENA*	
Offset 0x12 0FE8			*STB_DMAINTCLR*	
Offset 0x12 0FEC			*STB_DMAINTSET*	
Offset 0x12 0FF4			*POWERDOWN*	
Offset 0x12 0FFC			*MODULEID*	

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MSP 3 Registers

(PNX8526 User Manual, Ref. UM10104_1, Chap.33)

MSP 3 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
MSP 3 Registers begin at 0x12 8000. They are identical to the MSP 1 registers, described above. Note that MSP 3 does NOT implement the ICAM.				
Data Queue N (N=0 to 47) Head Pointer Registers				
Offset 0x12 8000—80BC			*DQHDPTR*	
Offset 0x12 80D0			*DQHDPTRBASE*	
Data Queue Interrupt Mask Registers				
Offset 0x12 80D4			*DQI0MSKHI*	
Offset 0x12 80D8			*DQI0MSKLO*	
Offset 0x12 80DC			*DQI1MSKHI*	
Offset 0x12 80E0			*DQI1MSKLO*	
Data Queue Interrupt Status Registers				
Offset 0x12 80E4			*DQISTATHI*	
Offset 0x12 80E8			*DQISTATLO*	
Data Queue Interrupt Threshold Registers				
Offset 0x12 80F0			*DQTHRESH0*	
Offset 0x12 80F4			*DQTHRESH1*	
Offset 0x12 80F8			*DQTHRESH2*	
Data Queue Control Registers				
Offset 0x12 80FC			*DQCTL*	
GP/HS Registers				
Offset 0x12 8100			*GPHSCTL*	
Offset 0x12 8104			*PKTSIZE*	
Offset 0x12 8108			*INSTHRESH*	
Offset 0x12 8110			*INSSTAT*	
Offset 0x12 8114			*INSCOUNT*	
Offset 0x12 8118			*PKTADDR*	
Offset 0x12 811C			*PKTDATA*	
Packet Framer Registers				
Offset 0x12 8200			*FRMRCTL*	
Offset 0x12 8204			*FRMRSYNC*	
Offset 0x12 8208			*PIDMASK*	
Offset 0x12 820C			*PIDCTL*	
Offset 0x12 8210			*PEAKVAL*	
Offset 0x12 8214—8258			*Reserved*	
DSS Bit Rate Registers				
Offset 0x12 825C			*DSS_BITRATE*	
Offset 0x12 8300—83FC			*PIDTABLE*	
RISC Engine Registers				

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MSP 3 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x12 8400			*RISCDBG0*	
Offset 0x12 8404			*RISCDBG1*	
Offset 0x12 8408			*RISCDBG2*	
Offset 0x12 840C			*RISCDBG3*	
Offset 0x12 8410			*RISCDBG4*	
Offset 0x12 8414			*RISCDBG5*	
Offset 0x12 8418			*RISCDBG6*	
Offset 0x12 841C			*RISCDBG7*	
Offset 0x12 8420			*RISCDBG8*	
Offset 0x12 8424			*RISCDBG9*	
Offset 0x12 8428			*RISCDBG10*	
Offset 0x12 842C			*RISCDBG11*	
Offset 0x12 8430			*RISCCTL*	
Offset 0x12 8434			*HSFCTL*	
De-Scrambler Keys				
*Offset 0x12 8600 + n*8*			*KEYnEVN0 (n = 0 to F)*	
*Offset 0x12 8604 + n*8*			*KEYnEVN1 (n = 0 to F)*	
*Offset 0x12 8680 + n*8*			*KEYnODD0 (n = 0 to F)*	
*Offset 0x12 8684 + n*8*			*KEYnODD1 (n = 0 to F)*	
Multi-2 Keys				
Offset 0x12 8700			*M2SYSKEY0*	
Offset 0x12 8704			*M2SYSKEY1*	
Offset 0x12 8708			*M2SYSKEY2*	
Offset 0x12 870C			*M2SYSKEY3*	
Offset 0x12 8710			*M2SYSKEY4*	
Offset 0x12 8714			*M2SYSKEY5*	
Offset 0x12 8718			*M2SYSKEY6*	
Offset 0x12 871C			*M2SYSKEY7*	
Copy Protect Keys				
Offset 0x12 8720			*CPKEYEVEN0*	
Offset 0x12 8724			*CPKEYEVEN1*	
Offset 0x12 8728			*CPKEYODD0*	
Offset 0x12 872C			*CPKEYODD1*	
De-Scrambler/Copy Protect Initialization Vectors				
Offset 0x12 8730			*DSCIVCBC0*	
Offset 0x12 8734			*DSCIVCBC1*	
Offset 0x12 8738			*DSCIVOFB0*	
Offset 0x12 873C			*DSCIVOFB1*	
Offset 0x12 8740			*CPIVCBC0*	

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MSP 3 REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x12 8744			*CPIVCBC1*	
Offset 0x12 8748			*CPIVOFB0*	
Offset 0x12 874C			*CPIVOFB1*	
De-Scrambler Modes				
Offset 0x12 8750			*MODEPAD*	
Offset 0x12 8754			*Reserved*	
Offset 0x12 8758			*Reserved*	
PI Bus Configuration Registers				
Offset 0x12 8C00			*MSPRST*	
MSP Interrupt Registers				
Offset 0x12 8FE0			*STB_DMAINTST*	
Offset 0x12 8FE4			*STB_DMAINTENA*	
Offset 0x12 8FE8			*STB_DMAINTCLR*	
Offset 0x12 8FEC			*STB_DMAINTSET*	
Offset 0x12 8FF4			*POWERDOWN*	
Offset 0x12 8FFC			*MODULEID*	

TPI Null 3 Module Registers

TPI NULL 3 MODULE REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x13 0FFC			*Module ID Register*	
31:16	R	0x0124	MOD_ID	Module ID Number
15:12	R	0	REV_MAJOR	Major revision
11:8	R	0	REV_MINOR	Minor revision
7:0	R	0xCF	APP_SIZE	Aperture size is 0 = 4 kB.

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Chapter 7: SPY Micro-Architecture

Programmable Source Decoder with Integrated Peripherals

Rev. 01 — 8 October 2003

7.1 Introduction

To aid in debugging DVP silicon, a SPY micro-architecture methodology has been used. The purpose of SPY micro-architecture is to allow important signals from each core (SPY signals) to be observed at specific chip pins. These signals provide functional data from each module to assist in debugging the chip.

The function of DVP SPY micro-architecture is to connect the SPY signals of each module to a multiplexer tree, which is then connected to functional chip pins at the top level. The SPY micro-architecture is controlled from several MMIO registers so that a specific PI-Bus master, with appropriate access rights, is able to control which SPY signals are routed to the top level SPY outputs. These MMIO registers are also accessible at an external debugger using the standardized JTAG interface.

7.2 SPY Micro-Architecture: Top Level

The basic topology chosen for the SPY micro-architecture is the binary tree. In this topology each module is connected to a leaf of a binary tree of 2-to-1 multiplexers (see Figure 1)

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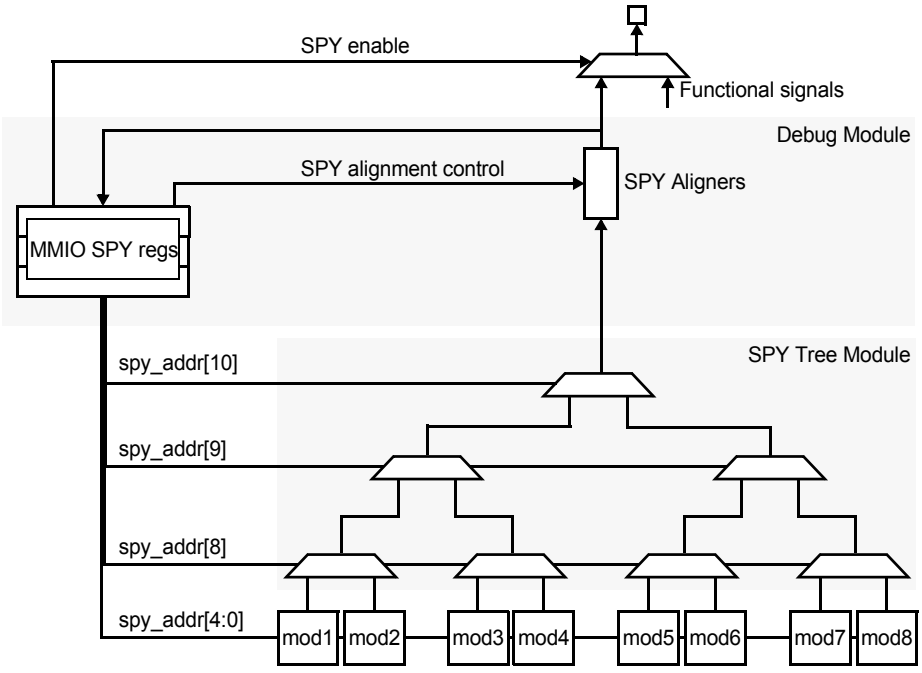

Figure 1: SPY micro-architecture

The SPY address is provided by the MMIO SPY control register DBG_SPY_ADDR_REG. The SPY output signals can be captured in the MMIO SPY data register DBG_SPY_DATA_REG. These registers are accessible to a bus master with appropriate access rights. They may also be accessed by an external debugger using the JTAG interface.

The SPY signals are multiplexed onto functional outputs when the spy_enable bit in the SPY control register DBG_SPY_ADDR_REG is set. Before the SPY signals are output, a programmable delay is introduced in each of the SPY lines to compensate for the skew each SPY signal is subject to in the SPY multiplexer tree. This delay is programmed in one of the MMIO SPY alignment registers DBG_SPY_ALIGN_REG0 or DBG_SPY_ALIGN_REG1.

7.2.1 SPY Outputs

The PNX8525 uses the digital video output of the second Image Composition Processor (ICP2) and some of the Audio Output pins for the real-time SPY outputs. Table 1 details the function of the internal SPY signals and their mapping onto functional chip pins in debug mode i.e., when the spy_enable bit in the DBG_SPY_ADDR_REG register is set.

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Table 1: Mapping of SPY Signals onto Chip Output Pins

Signal	Output Pin	Function	Pad Type
spy_out[9:0]	DV_OUT2[9:0]	Core SPY signals	PDT08DGZ
spy_out[10]	I2S_OUT2_SCK	Core SPY signal	PDU08SDGZ
spy_out[11]	I2S_OUT2_OSCLK	Local reference clock	PDT08DGZ
clk_spy	I2S_OUT2_SD	Global SPY reference clock	PDT04DGZ

Remark: In order not to lose too much timing accuracy in the SPY signals, special care has to be taken in routing the signals from these pins to the logic analyzer connector on the prototype board. The capacitive load on these pins has to be minimized.

The two SPY signals spy_out[11] and clk_spy contain synchronization information to relate the SPY outputs to a certain absolute time interval and to their local clock. The purpose of these signals is described in more detail in Section 7.4.

7.2.2 SPY Module Addressing

The SPY module addressing scheme works with a global SPY address bus, which is controlled from the MMIO SPY control register and connects to all the modules and top-level multiplexers (see Figure 1). The selection of a particular module is achieved by writing its SPY address into this register.

The PNX8525 SPY micro-architecture uses a 9-bit wide global SPY address to address each module. Complex modules can output more SPY sets by using five additional local address bits inside the module to select one SPY set out of a maximum of 32 sets of 12 SPY signals. To allow future extensions, the maximum number of local SPY address bits has been set to 8, which makes the total number of SPY address bits 17.

The actual SPY address for each module depends on the placement and routing constraints and is determined afterwards by the debugger software. More information on this procedure can be found in Section 7.5 and Section 7.8.6.

7.2.3 MMIO SPY Registers

The MMIO registers used to control the SPY micro-architecture are located in the debug module. An abstract from the Debug Design Specification [1] is provided below, showing the layout of the SPY related registers.

SPY MICRO-ARCHITECTURE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x04 1000			*DBG_SPY_ADDR_REG*	
31	W	0	spy_enable	If 1, SPY signals are sent to the designated chip output pins
30	W	0	mips_pc_trace_enable	If 1, MIPS PC trace signals are multiplexed onto the SPY outputs
29:17	R	NI	Reserved	Read as 0.
16:0	R/W	0	spy_addr	17-bit SPY micro-architecture address
Offset 0x04 1004			*DBG_SPY_DATA_REG*	

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SPY MICRO-ARCHITECTURE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
31:12	R	NI	Reserved	Read as 0.
11:0	R	0	spy_data[11:0]	Contains the value of the 12 SPY outputs sampled on the PI-Bus clock.
Offset 0x04 1008			*DBG_SPY_ALIGN_REG0*	
31:28	R/W	0x0	spy_align7[3:0]	SPY alignment control for SPY signal 7 (spy_out[7]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay
27:24	R/W	0x0	spy_align6[3:0]	SPY alignment control for SPY signal 6 (spy_out[6]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay
23:20	R/W	0x0	spy_align5[3:0]	SPY alignment control for SPY signal 5 (spy_out[5]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay

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SPY MICRO-ARCHITECTURE REGISTERS				
Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
19:16	R/W	0x0	spy_align4[3:0]	SPY alignment control for SPY signal 4 (spy_out[4]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay
15:12	R/W	0x0	spy_align3[3:0]	SPY alignment control for SPY signal 3 (spy_out[3]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay
11:8	R/W	0x0	spy_align2[3:0]	SPY alignment control for SPY signal 2 (spy_out[2]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay

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SPY MICRO-ARCHITECTURE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
7:4	R/W	0x0	spy_align1[3:0]	SPY alignment control for SPY signal 1 (spy_out[1]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay
3:0	R/W	0x0	spy_align0[3:0]	SPY alignment control for SPY signal 0 (spy_out[0]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay
Offset 0x04 100C			*DBG_SPY_ALIGN_REG1*	
31:16	R	NI	reserved	Read as 0.
15:12	R/W	0x0	spy_align11[3:0]	SPY alignment control for SPY signal 11 (spy_out[11]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay

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SPY MICRO-ARCHITECTURE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
11:8	R/W	0x0	spy_align10[3:0]	SPY alignment control for SPY signal 10 (spy_out[10]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay
7:4	R/W	0x0	spy_align9[3:0]	SPY alignment control for SPY signal 9 (spy_out[9]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay
3:0	R/W	0x0	spy_align8[3:0]	SPY alignment control for SPY signal 8 (spy_out[8]) 0x0 = 0 DLY4X1 cell delay 0x1 = 2 DLY4X1 cell delay (approx. 2.2 ns) 0x2 = 4 DLY4X1 cell delay 0x3 = 6 DLY4X1 cell delay 0x4 = 8 DLY4X1 cell delay 0x5 = 10 DLY4X1 cell delay 0x6 = 12 DLY4X1 cell delay 0x7 = 14 DLY4X1 cell delay 0x8 = 10 DLY4X1 cell delay 0x9 = 12 DLY4X1 cell delay 0xA = 14 DLY4X1 cell delay 0xB = 16 DLY4X1 cell delay 0xC = 18 DLY4X1 cell delay 0xD = 20 DLY4X1 cell delay 0xE = 22 DLY4X1 cell delay 0xF = 24 DLY4X1 cell delay
Offset 0x04 1FF4			*Powerdown Register*	
31	R/W	0	POWER_DOWN	Powerdown indicator 1 = Powerdown 0 = Power up When this bit equals 1, no other registers are accessible.
30:0		-	Unused	

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SPY MICRO-ARCHITECTURE REGISTERS				
Bits	**Read/ Write**	**Reset Value**	**Name (Field or Function)**	**Description**
Offset 0x04 1FFC			*Module ID Register*	
31:16	R	0116	MOD_ID	Module ID Number
15:12	R	0	REV_MAJOR	Major revision
11:8	R	0	REV_MINOR	Minor revision
7:0	R	00	APP_SIZE	Aperture size is 0 = 4 kB.

The DBG_SPY_CTRL_REG is used to address the SPY modules. It also contains an additional spy_enable bit to multiplex the top-level SPY outputs to the functional pins, thereby enabling the SPY micro-architecture (see Figure 1). Furthermore a mips_pc_trace_enable bit is available to multiplex the MIPS PC trace signals onto the SPY outputs.

The DBG_SPY_DATA_REG is used to observe the SPY bus from software. Its main purpose is to read the module identification number using debugger software running on an embedded processor or external host. For all SPY addresses it samples the current state of the 12 top-level SPY signals on the PI-Bus clock.

If the JTAG interface is used to capture the SPY signals, they are captured on the positive edge of the JTAG clock and can be serially shifted out through the JTAG port.

The DBG_SPY_ALIGN_REG0/1 registers are used to program the SPY aligners. These aligners introduce a specific delay in each of the SPY lines, which allows the SPY signals to be lined up on an external logic analyzer display.

7.3 SPY Micro-Architecture: Module Level

Standard SPY library modules have been designed that can be easily plugged into the individual DVP modules. The implementation of these library modules is described in Section 7.8.

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The figure below shows how a SPY library module is added to a DVP module.

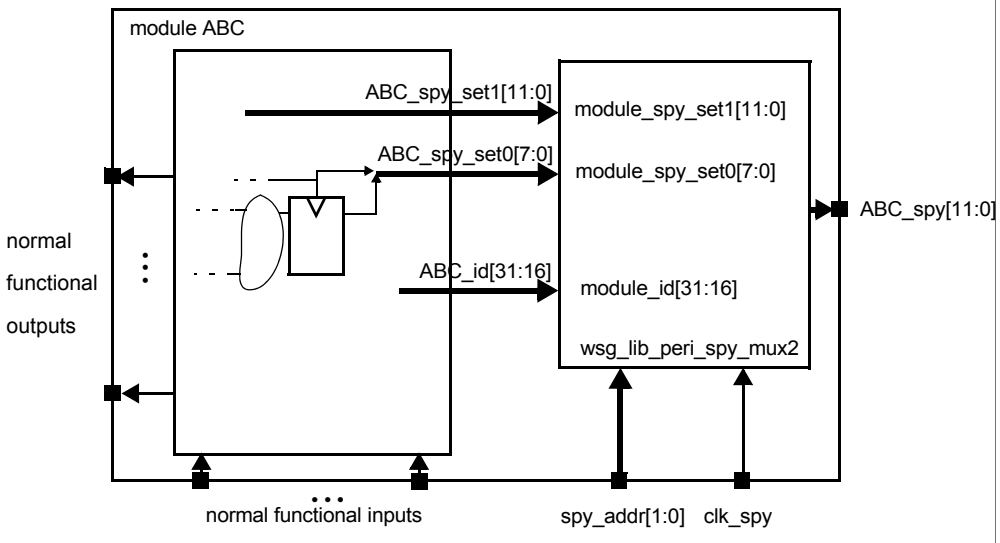

Figure 1: SPY Micro-Architecture at Module Level

In the above figure, a DVP module called ABC with 20 SPY signals is shown. The SPY signals of this module have been split over two SPY sets of 8 and 12 signals. These sets (together with the mandatory module identification number) are multiplexed to one set of 12 SPY signals using one of the standard SPY multiplexer modules. The resulting 12 SPY signals are called ABC_spy[11:0] to reflect their origin.

In this example, SPY address 0 will select the12 LSBits of the PNX8525 ABC module ID (ABC_id[27:16]), and SPY address 1 will select the remaining 4 MSbits of the ID, combined with the eight SPY signals from the module itself (ABC_spy_set0[7:0] and ABC_id[31:28]).

SPY address 2 will select 12 synchronized copies of the SPY timing clock (clk_spy), which will allow the actual delay in the SPY paths to be determined for each module in the SPY tree. More information on this procedure can be found in Section 7.4. SPY address 3 contains the remaining 12 SPY signals (ABC_spy_set1[11:0]).

As shown in Figure 1, adding the standard SPY multiplexer module to a DVP module involves adding three terminals to that module's interface as follows:

- SPY address (spy_addr[4:0] or a subset thereof)
- SPY timing clock (clk_spy)
- 12 SPY outputs (<module>_spy[11:0])

7.4 SPY Timing and Accuracy

The global time-stamping clock is used to time-stamp events in the GPIO module and is normally never stopped. The SPY timing clock is derived from this time-stamp clock in the clocks module. The SPY clock is used in the SPY micro-architecture to

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provide both an absolute time reference and a means of measuring the individual delays of SPY signals in the SPY micro-architecture. Measuring these delays and compensating for them provides a more accurate comparison between the SPY signals.

The SPY clock is directly routed to the I2S_OUT2_SCK output pin in SPY mode (i.e., when spy_enable is asserted). It is also routed to each of the DVP modules. In each module it is expanded to a set of 12 SPY signals that is output when SPY address 2 is selected (see Figure 1).

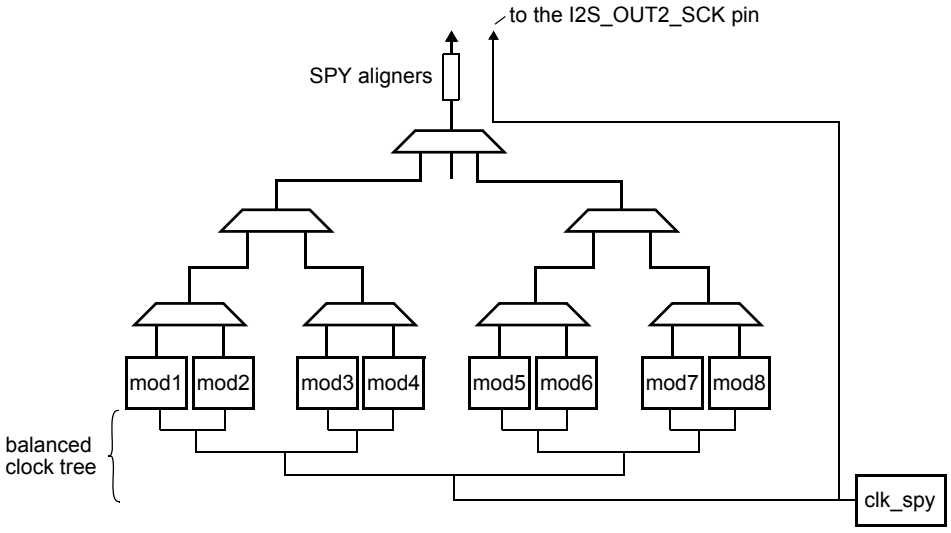

Figure 1: SPY Clock Usage in the SPY Micro-Architecture

As this entire clock tree is balanced, it allows the delays of the individual SPY signals to be compared to the clock signal output on pin I2S_OUT2_SCK. A delay that a SPY signal may encounter when passing through the SPY micro-architecture can be compensated by using the programmable SPY aligners.

The SPY alignment settings that are obtained for the clock set can be reused for the other SPY sets in the same module. The worst-case inaccuracy that can result from reusing these measured delays is approximately 2-3ns, depending on wire-load differences inside the module.

To align the SPY outputs, special SPY aligner modules are used. This module is instantiated in the signal line for every SPY signal before it is output (see Figure 2).

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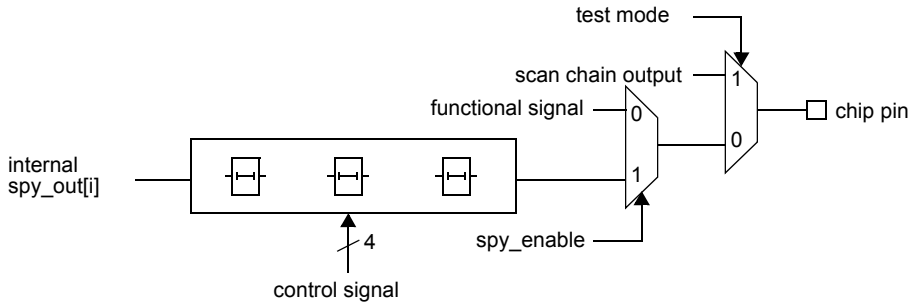

Figure 2: SPY Signal Alignment

During test mode the test block will control the output signal on the chip pin to allow production testing. During functional mode i.e.when the test block is in reset, the spy_enable signal from the Debug module [1] can overrule the functional output signal and output the SPY signal instead.

The SPY aligner allows each SPY signal to be individually delayed in steps of approx. 2ns, up to a total delay of approx. 24 ns (worst case). By default, the aligners are set to bypass all the delay elements.

Based on the results obtained from the clk_spy set, individual delays can be adjusted to line up the SPY signals. Please refer to Section 7.8.7 for the full specification of the SPY alignment module.

7.5 Debugger Software Support

The debugger software takes care of determining the precise relation between the SPY module and its SPY addresses on silicon. It does this by traversing the SPY address space while selecting SPY sets 0 and 1 for each module. This will output the module identification number of all DVP modules connected to the SPY micro-architecture. Given the implementation presented in Section 7.3 this can be fully automated. The debugger software can run on one of the processors inside the PNX8525 or, as access is also possible through the JTAG port, on any host PC with a JTAG interface.

Remark: The identification for each module is restricted to module type identification only. Instantiations of the same type cannot be distinguished from one another by only using the SPY micro-architecture. Determining the instantiation is possible however by accessing a particular instantiation via the PI-Bus and monitoring that access via the SPY micro-architecture.

7.6 Application

Typical application of the SPY mechanism is to first determine the mapping of a PNX8525 module to a SPY address and next, to determine the delay for each of the 12 synchronized SPY clock signals. These will be used to compensate the delay of any signal originating from the same module with the same SPY set index.

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Remark: For the example shown in Figure 1, ABC_spy_set0[7] will use the same delay compensation as ABC_spy_set1[11], as both are multiplexed onto the same SPY output signal (ABC_spy[11]).

The SPY micro-architecture with appropriate address mapping and delay figures can then be used in helping to debug the device.

7.7 Testability

The SPY micro-architecture will be tested during production using a special functional test. Before a debug session is started, the debug software performs a more extensive test on the SPY hardware.

7.8 Standard SPY Modules

7.8.1 Two-SPY Set Multiplexer Module

Figure 1 shows a SPY module that allows two SPY sets to be multiplexed onto the SPY micro-architecture. Table 2 describes the behavior of this module.

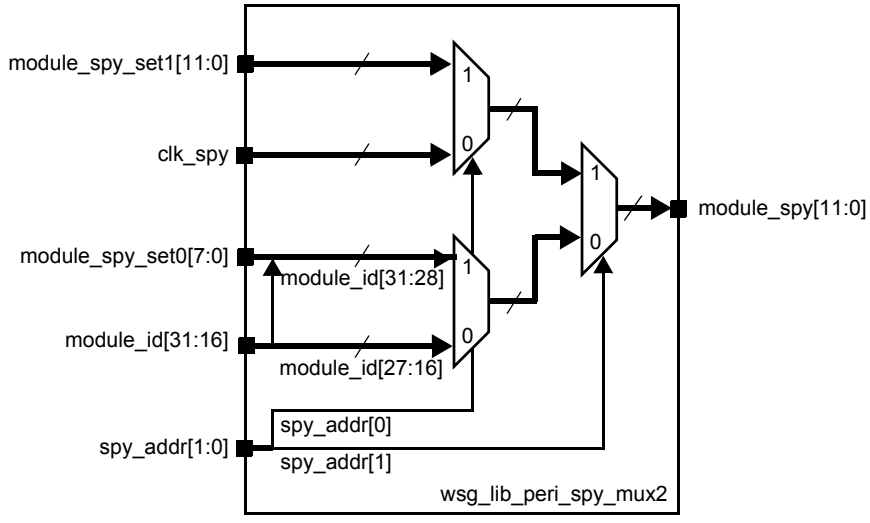

Figure 1: Standard Two-SPY Set Multiplexer Module

Table 2: Behavior of Two-SPY Set Multiplexer Module

spy_addr[1:0]	module_spy[11:0]	Signal Description
00b	module_id[27:16]	12 LSBits of the PNX8525 module ID
01b	module_spy_set0[7:0], module_id[31:28]	SPY set 0 (8 SPY signals, MSB is clock), 4 MSBits of the PNX8525 module ID
10b	clk_spy	Clock used for timing measurements
11b	module_spy_set1[11:0]	SPY set 1 (12 SPY signals, MSB is clock)

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7.8.2 Four-SPY Set Multiplexer Module

Table 1 shows a SPY module that allows four SPY sets to be multiplexed onto the SPY micro-architecture. Table 3 describes the behavior of this module.

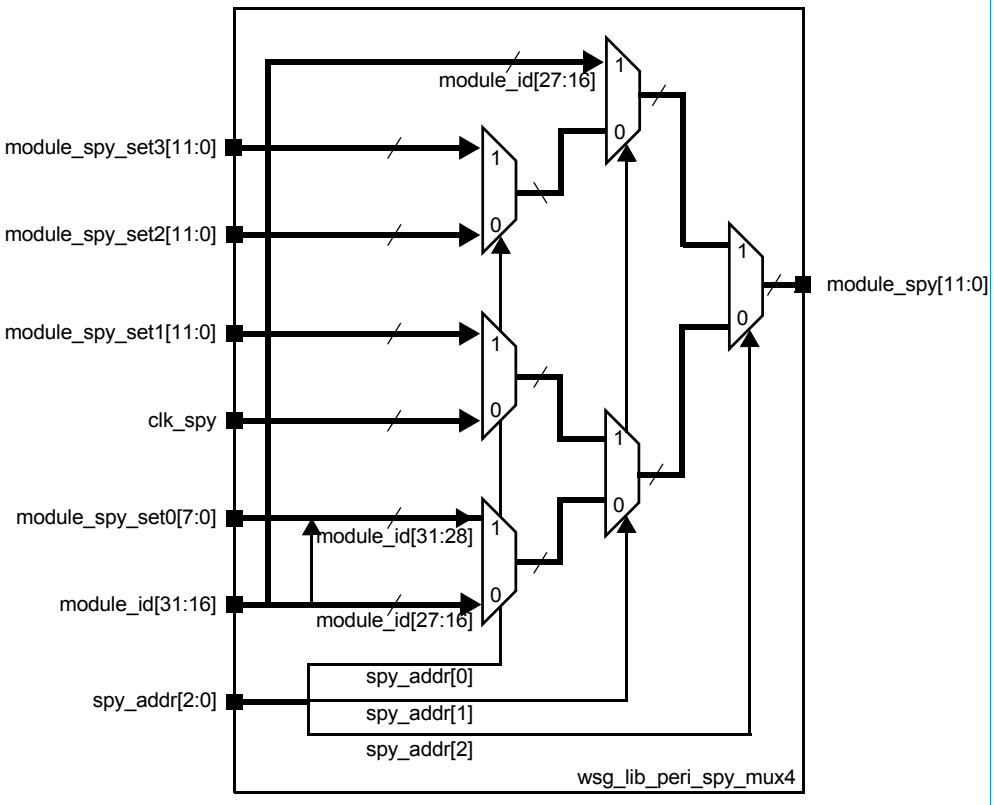

Figure 1: Standard Four-SPY Set Multiplexer Module

Table 3: Behavior of the Four-SPY Set Multiplexer Module

spy_addr[2:0]	module_spy[11:0]	Signal Description
000b	module_id[27:16]	12 LSBits of the PNX8525 module ID
001b	module_spy_set0[7:0], module_id[31:28]	SPY set 0 (8 SPY signals, MSB is clock), 4 MSBits of the PNX8525 module ID
010b	clk_spy	Clock used for timing measurements
011b	module_spy_set1[11:0]	SPY set 1 (12 SPY signals, MSB is clock)
100b	module_spy_set2[11:0]	SPY set 2 (12 SPY signals, MSB is clock)
101b	module_spy_set3[11:0]	SPY set 3 (12 SPY signals, MSB is clock)
110b	module_id[27:16]	12 LSBits of PNX8525 module ID
111b	module_id[27:16]	12 LSBits of PNX8525 module ID

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7.8.3 Six-SPY Set Multiplexer Module

Figure 1 shows a SPY module that allows six SPY sets to be multiplexed onto the SPY micro-architecture. Table 4 describes the behavior of this module.

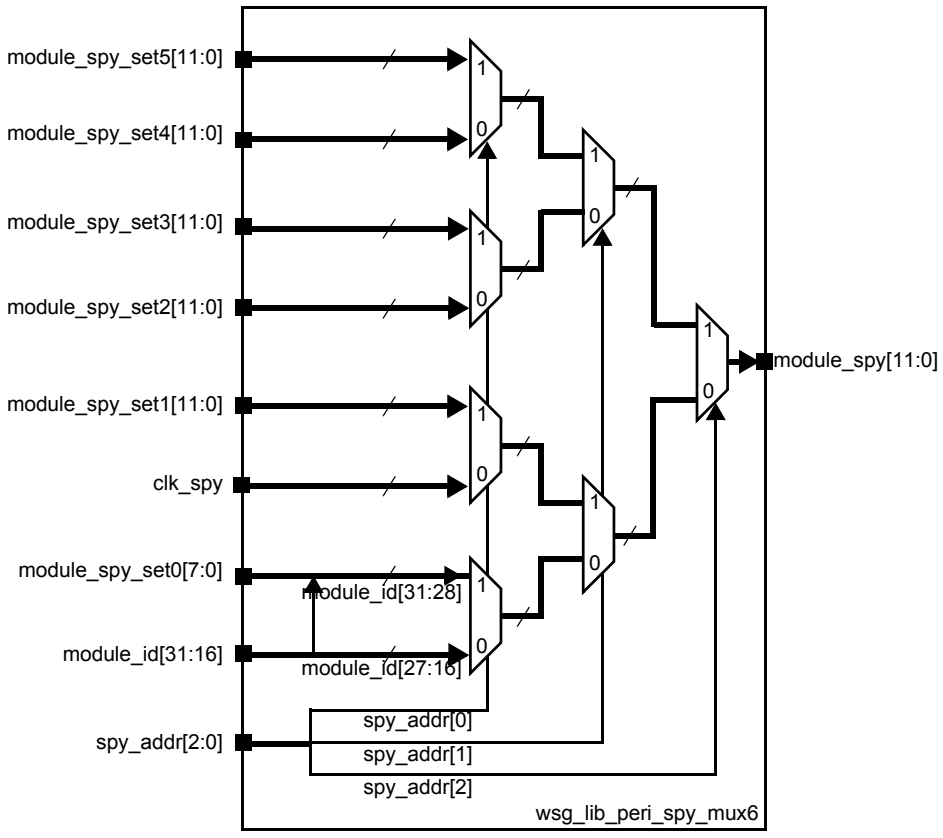

Figure 1: Standard Six-SPY Set Multiplexer Module

Table 4: Behavior of the Six-SPY Set Multiplexer Module

spy_addr[2:0]	module_spy[11:0]	Signal Description
000b	module_id[27:16]	12 LSBits of the PNX8525 module ID
001b	module_spy_set0[7:0], module_id[31:28]	SPY set 0 (8 SPY signals, MSB is clock), 4 MSBits of the PNX8525 module ID
010b	clk_spy	Clock used for timing measurements
011b	module_spy_set1[11:0]	SPY set 1 (12 SPY signals, MSB is clock)
100b	module_spy_set2[11:0]	SPY set 2 (12 SPY signals, MSB is clock)
101b	module_spy_set3[11:0]	SPY set 3 (12 SPY signals, MSB is clock)
110b	module_spy_set4[11:0]	SPY set 4 (12 SPY signals, MSB is clock)
111b	module_spy_set5[11:0]	SPY set 5 (12 SPY signals, MSB is clock)

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7.8.4 Nine-SPY Set Multiplexer Module

Figure 1 shows a SPY module that allows nine SPY sets to be multiplexed onto the SPY micro-architecture. Table 5 describes the behavior of this module.

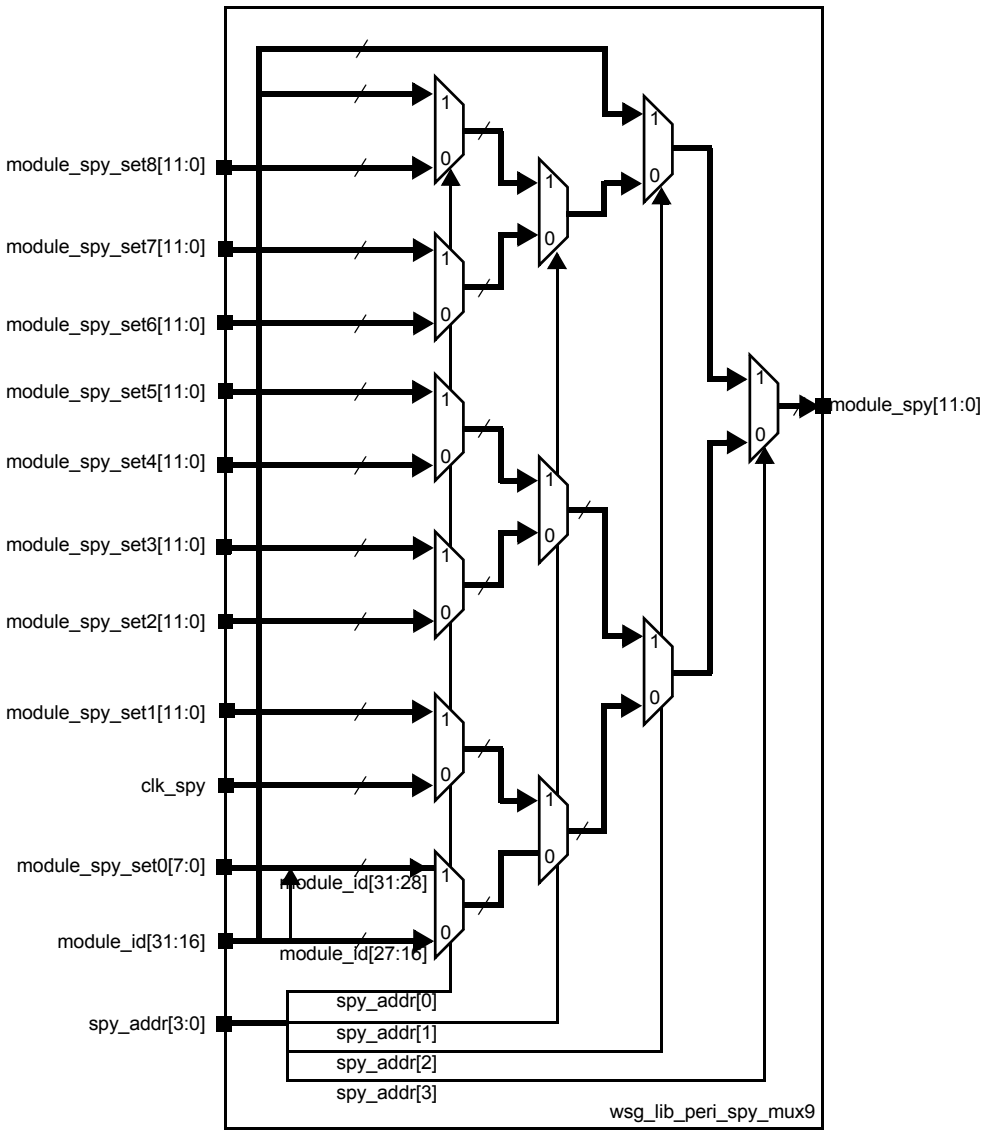

Figure 1: Nine-SPY Set Multiplexer Module

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Table 5: Behavior of the Nine-SPY Set Multiplexer Module

spy_addr[3:0]	module_spy[11:0]	Signal Description
0000b	module_id[27:16]	12 LSBits of the PNX8525 module ID
0001b	module_spy_set0[7:0], module_id[31:28]	SPY set 0 (8 SPY signals, MSB is clock), 4 MSBits of the PNX8525 module ID
0010b	clk_spy	Clock used for timing measurements
0011b	module_spy_set1[11:0]	SPY set 1 (12 SPY signals, MSB is clock)
0100b	module_spy_set2[11:0]	SPY set 2 (12 SPY signals, MSB is clock)
0101b	module_spy_set3[11:0]	SPY set 3 (12 SPY signals, MSB is clock)
0110b	module_spy_set4[11:0]	SPY set 4 (12 SPY signals, MSB is clock)
0111b	module_spy_set5[11:0]	SPY set 5(12 SPY signals, MSB is clock)
1000b	module_spy_set6[11:0]	SPY set 6(12 SPY signals, MSB is clock)
1001b	module_spy_set7[11:0]	SPY set 7 (12 SPY signals, MSB is clock)
1010b	module_spy_set8[11:0]	SPY set 8(12 SPY signals, MSB is clock)
1011b	module_id[27:16]	12 LSBits of the DVP3218 module ID
1100b	module_id[27:16]	12 LSBits of the DVP3218 module ID
1101b	module_id[27:16]	12 LSBits of the DVP3218 module ID
1110b	module_id[27:16]	12 LSBits of the DVP3218 module ID
1111b	module_id[27:16]	12 LSBits of the DVP3218 module ID

7.8.5 Fourteen-SPY Set Multiplexer Module

Figure 1 shows a SPY module that allows 14 SPY sets to be multiplexed onto the SPY micro-architecture. Table 6 describes the behavior of this module.

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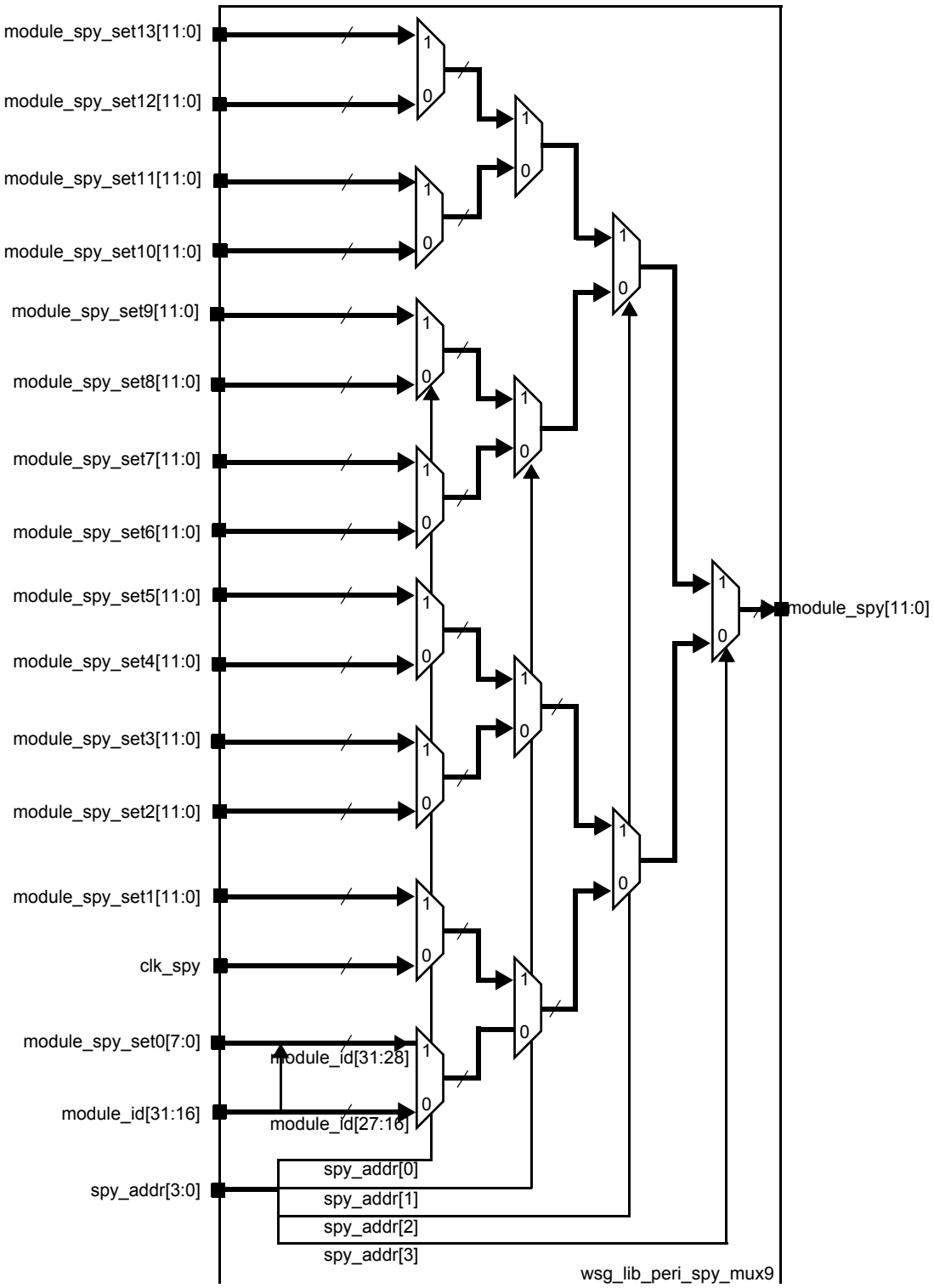

Figure 1: Fourteen-SPY Set Multiplexer Module

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Table 6: Behavior of Fourteen-SPY Set Multiplexer Module

spy_addr[3:0]	module_spy[11:0]	Signal Description
0000b	module_id[27:16]	12 LSBits of the PNX8525 module ID
0001b	module_spy_set0[7:0], module_id[31:28]	SPY set 0 (8 SPY signals, MSB is clock), 4 MSBits of PNX8525 module ID
0010b	clk_spy	Clock used for timing measurements
0011b	module_spy_set1[11:0]	SPY set 1 (12 SPY signals, MSB is clock)
0100b	module_spy_set2[11:0]	SPY set 2 (12 SPY signals, MSB is clock)
0101b	module_spy_set3[11:0]	SPY set 3 (12 SPY signals, MSB is clock)
0110b	module_spy_set4[11:0]	SPY set 4 (12 SPY signals, MSB is clock)
0111b	module_spy_set5[11:0]	SPY set 5 (12 SPY signals, MSB is clock)
1000b	module_spy_set6[11:0]	SPY set 6 (12 SPY signals, MSB is clock)
1001b	module_spy_set7[11:0]	SPY set 7 (12 SPY signals, MSB is clock)
1010b	module_spy_set8[11:0]	SPY set 8 (12 SPY signals, MSB is clock)
1011b	module_spy_set9[11:0]	SPY set 9 (12 SPY signals, MSB is clock)
1100b	module_spy_set10[11:0]	SPY set 10 (12 SPY signals, MSB is clock)
1101b	module_spy_set11[11:0]	SPY set 11 (12 SPY signals, MSB is clock)
1110b	module_spy_set12[11:0]	SPY set 12 (12 SPY signals, MSB is clock)
1111b	module_spy_set13[11:0]	SPY set 13 (12 SPY signals, MSB is clock)

7.8.6 Top Level SPY Tree Modules

At the top level, SPY outputs of 48 modules are multiplexed onto a single set of 12 SPY signals. The architecture is split into individual submodules to facilitate top-level partitioning and routing. The implementation of the top-level SPY tree module is shown in Figure 1.

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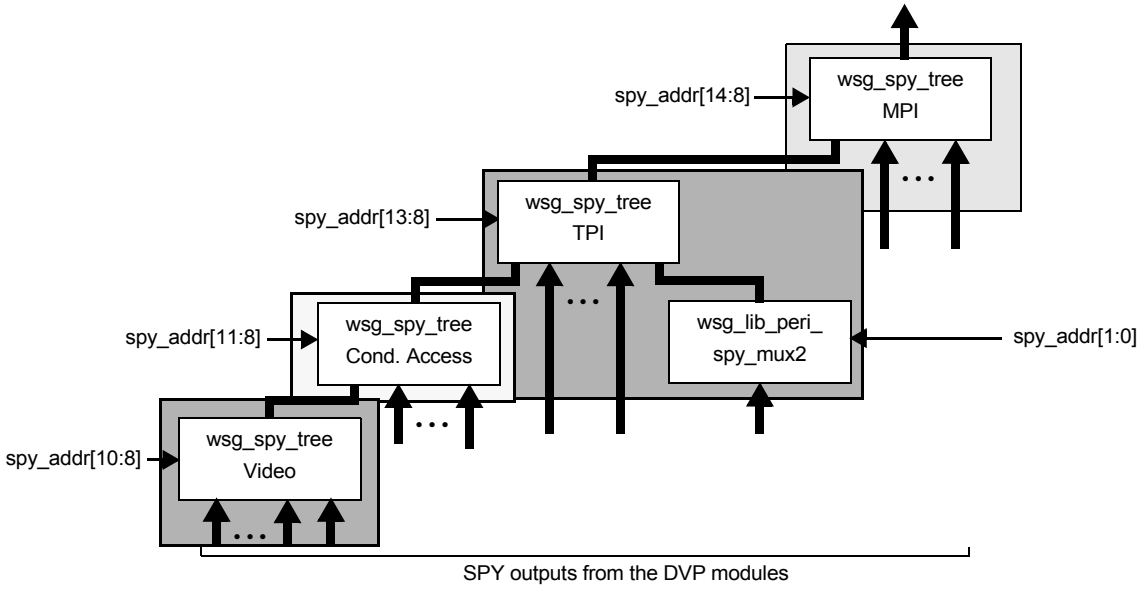

Figure 1: PNX8525 Top-Level SPY Multiplexing

[6-1] The shaded backgrounds indicate the chiplet partitioning.

Table 7 shows the partitioning of the PNX8525 modules over the various chiplets, and their SPY address in the SPY micro-architecture.

Table 7: Chiplet Allocation/Base SPY Addrs. PNX8525 Modules

Module	Chiplet	Base SPY Address
dtv_vmpg	dtv_vmpg	0x0000
wsg_vip1	video	0x0400
wsg_vip2	video	0x0500
wsg_mbs	video	0x0600
wsg_msp1	caccess	0x0800
wsg_msp2	caccess	0x0900
wsg_ssi	tpi	0x1000
dtv_ai1	tpi	0x1100
dtv_ao1	tpi	0x1200
dtv_ai2	tpi	0x1300
dtv_ao2	tpi	0x1400
dtv_ai3	tpi	0x1500
dtv_ao3	tpi	0x1600
wsg_tpbc	tpi	0x1700
dtv_spdi	tpi	0x1800
wsg_gpio	tpi	0x1900
wsg_pimi	tpi	0x1A00

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Table 7: Chiplet Allocation/Base SPY Addrs. PNX8525 Modules *...Continued*

Module	Chiplet	Base SPY Address
wsg_pic	tpi	0x1C00
wsg_tsdma	tpi	0x1D00
dtv_spdo	tpi	0x1E00
wsg_pib	tpi	0x1F00
tm_3218	tm	0x2000
wsg_pib	mpi	0x4000
wsg_fpbc	mpi	0x4300
wsg_mpbc	mpi	0x4400
wsg_uart1	mpi	0x4500
wsg_uart2	mpi	0x4600
wsg_uart3	mpi	0x4700
wsg_pimi	mpi	0x4800
wsg_iic1	mpi	0x4A00
wsg_iic2	mpi	0x4B00
wsg_usb	mpi	0x4C00
wsg_boot	mpi	0x4D00
wsg_pimi	mpi	0x4E00
wsg_pci	mpi	0x4F00
wsg_dbg	mpi	0x5000
wsg_clocks	mpi	0x5100
wsg_pic	mpi	0x5200
wsg_reset	mpi	0x5300
wsg_glbreg2	mpi	0x5400
wsg_glbreg1	mpi	0x5500
stb_dma	mpi	0x5600
wsg_pib	mpi	0x5700

Remark: The position of a certain module in the SPY micro-architecture can be verified by setting its base SPY address in the DBG_SPY_ADDR_REG and reading back the module ID bits 27 through 16 using the DBG_SPY_DATA_REG (see Section 7.2.3).

Please refer to the chapter on each module for more details on which signals can be selected as SPY signals.

7.8.7 SPY Aligner Module

The SPY aligner module is used to add a programmable delay to each SPY signal, which is then used to compensate for the difference in propagation delay each signal is subjected to in the SPY tree. The SPY aligner module can add a programmable delay to each individual SPY signal of up to 24 DLY4X1 propagation delays, in increments of 2.

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Programmability is obtained by using a series of delay elements, optionally bypassed by multiplexers. The implementation of the SPY aligner module is shown in Figure 1. Based on the state of the control signal S[3:0] the delay caused by the delay elements may be added to the spy_in signal.

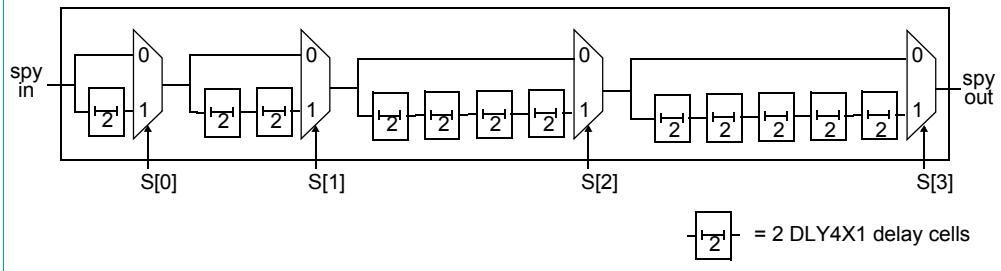

Figure 1: Programmable SPY Delay Element

Table 8: Delay Cell Characteristics

Delay Cell Characteristics (DLY4X1)	
Pin capacitance (typical)	0.0018 pF
Intrinsic delays (typical)	0.708 ns (A↑Y)
	0.648 ns (A↓Y)
Load delays (typical)	4.564 ns/pF (A↑Y)
	2.771 ns/pF (A↓Y)
Delay (typical)	0.7162 ns (A↑Y)
Delay (typical)	0.6530 ns (A↓Y)
Derating factor	1.63
Delay (worst case)	1.1674 ns (A↑Y)
Delay (worst case)	1.0644 ns (A↓Y)

Figure 2 shows the implementation of the SPY multiplexer/aligner module. It aligns the SPY signals from the top-level SPY tree module, and optionally multiplexes in the MIPS PC trace signals.

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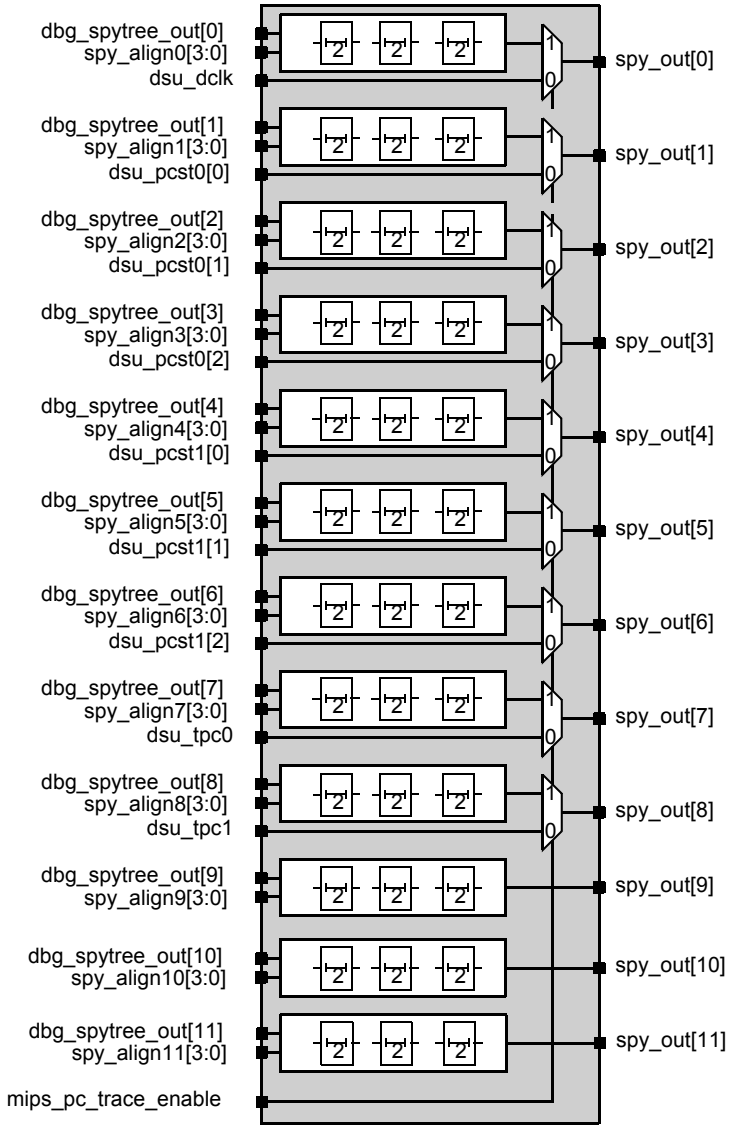

Figure 2: SPY Multiplex/Aligner Module

Ten basic SPY alignment modules are used to obtain a maximum delay of approximately 24 ns. The alignment control signals come from the DBG_SPY_ALIGN_REG0 and DBG_SPY_ALIGN_REG1 MMIO registers. These MMIO registers allow the delay for each SPY signal to be programmed from any privileged bus master or from an external debugger connected to the JTAG port.

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7.9 TM32 CPY Core SPY Signals

The intent of the TM32 CPU core SPY signals is to aid in debugging the core on silicon. Certain core internal signals are available through the tm32_core_spy[9:0] output pins of the TM32 core. The selection of what signals are output is controlled through bits in several MMIO registers (i.e.,unused bits in the MMIO registers of TM32 CPU blocks). The TM32 CPU core provides 10 SPY output bits, which are connected to the top-level PNX8525 SPY micro-architecture, using the standard two-SPY set multiplexer module (see Figure 1 for more details).

7.9.1 TM32 Core SPY Details

The SPY signals are internally “daisy chained” between the TM32 CPU core internal blocks. Figure 1 shows the daisy-chain of the SPY signals.

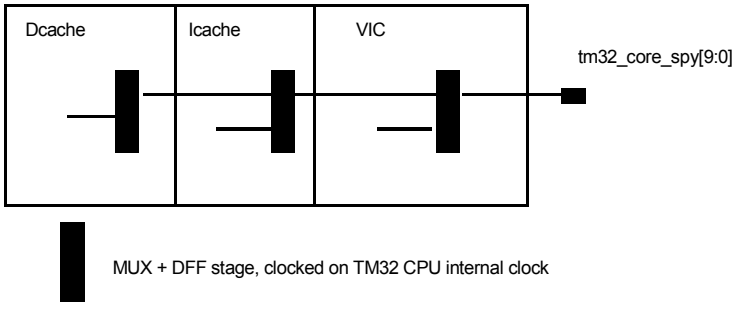

Figure 1: SPY Signal Daisychain in TM32 CPU Core

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7.9.2 D-Cache SPY Implementation

The D-Cache block does not receive any input SPY signals (see Figure 2)

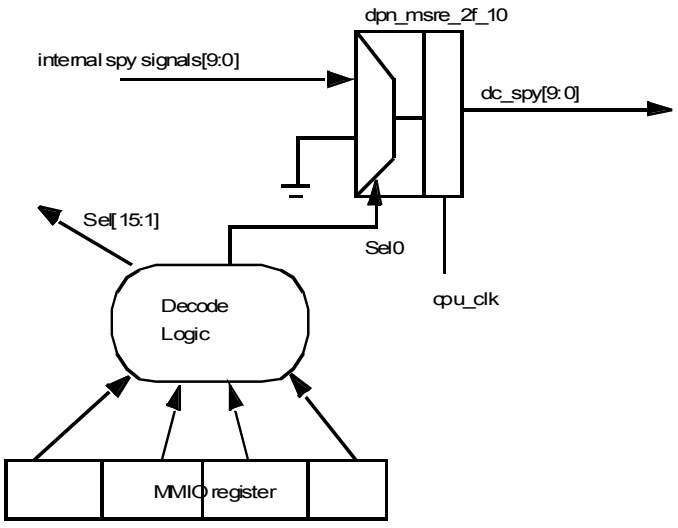

Figure 2: D-Cache SPY Implementation

7.9.3 I-Cache, VIC SPY Implementation

The I-Cache and VIC SPY implementation is shown in Figure 3.

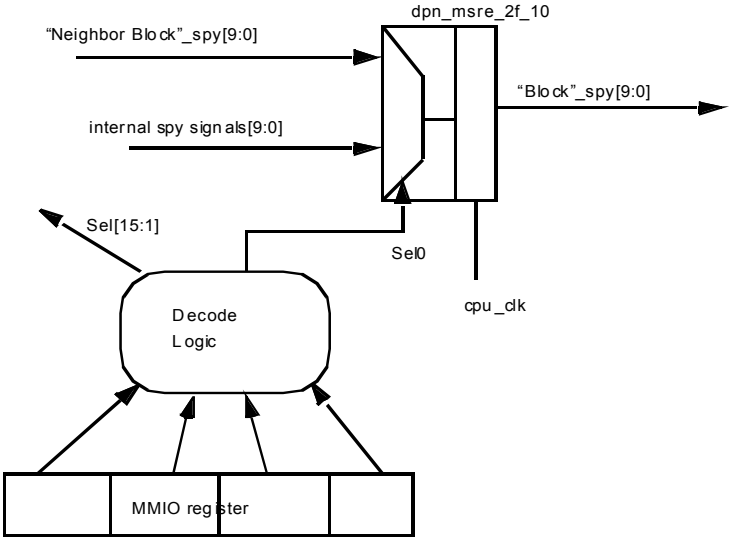

Figure 3: I-Cache and VIC SPY Implementation

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7.9.4 SPY MMIO Registers

The table below shows the TM32 CPU core MMIO registers that control the SPY signal MUX's.

Table 9: SPY MMIO Registers

BLOCK	REGISTER NAME	MMIO OFFSET	BITS	WIDTH
DCACHE	DC_LOCK_CTL	0x100010	4:1	4
ICACHE	IC_LOCK_CTL	0x100210	4:1	4
VIC	SYSTIMER_TCTL	0x100c68	23:20	4

7.9.5 D-Cache SPY Signals

Table 10: D-Cache SPY Signals

MMIO SPY Register Value	SPY Signals Selected [MSB:LSB]
0000 (reset default)	2'b0,dstall,cache_state,state_miss_fsm[5:0]
0001	1'b0, state_cb[2:0], state_lock_fsm[5:0]
0010	1'b0, state_cb_misr[2:0], state_fetch2[2:0],state_fetch3[2:0]
0100	5'b0,state_arbiter[4:0]

7.9.6 I-Cache SPY Signals

Table 11: I-Cache SPY Signals

MMIO SPY Register Value	SPY Signals Selected [MSB:LSB]
0000 (reset default)	pc_spy[9:0]
0001	pc_spy[19:10]
0010	pc_spy[29:20]
0011	selJplus4,selJplus0,state,istall_out,pc_spy[31:30]
0100	selLplus48, selLplus32, selLplus16, selLplus0, selKplus3, selKplus2, selKplus1, selKplus0, selJplus12, selJplus8
0101	selBisB_, selAisE_, selAisD_, selAisC_, selAisB_, sel5ext_, sel4ext_, sel3ext_, sel2ext_, sel1ext_
0110	enB[0], selEisE_, selDisE_, selDisD_, selCisE_, selCisD_, selCisC_, selBisE_, selBisD_, selBisC_
0111	enDD[2:0],enC[4:0],enB[2:1]
1000	enE[5:0],enDD[6:3]
1001	idataEn_[6:0],enE[8:6]
1010	no_branch2,idataEn_[15:7]
1011	pass dc_spy[9:0]

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7.9.7 VIC SPY Signals

Table 12: VIC SPY Signals

MMIO SPY Register Value	SPY Signals Selected [MSB:LSB]
0000 (reset default)	ic_spy[9:0]
0001	vic_cpu_intvec[9:0]
0010	vic_cpu_intvec[19:10]
0011	vic_cpu_intvec[29:20]
0100	4'b0,time_ireq[3:0], vic_cpu_intvec[31:30]

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